Sub-1GHz Wireless Module(DIP)

REX2DP

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VERSION HISTORY

V1.0.0	2010/06/4	1st issue of preliminary document

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1. Introduction

Rexense Sub-1GHz Wireless Module (REX2DP) is a type of surface mounted module that enables users to implement wireless solution which satisfies the needs of low-cost, low-power wireless sensor networks. The module is easy-to-use, saves board space and offers reliable delivery of data between devices.

Rexense Sub-1GHz Wireless Module (REX2DP) operates from ISM 240-960Mhz frequency band. The module's default configuration supports a wide range of data system applications. The module is embedded with 32-bit wireless microcontroller to offer a wide variety of solutions.

2. Product Features

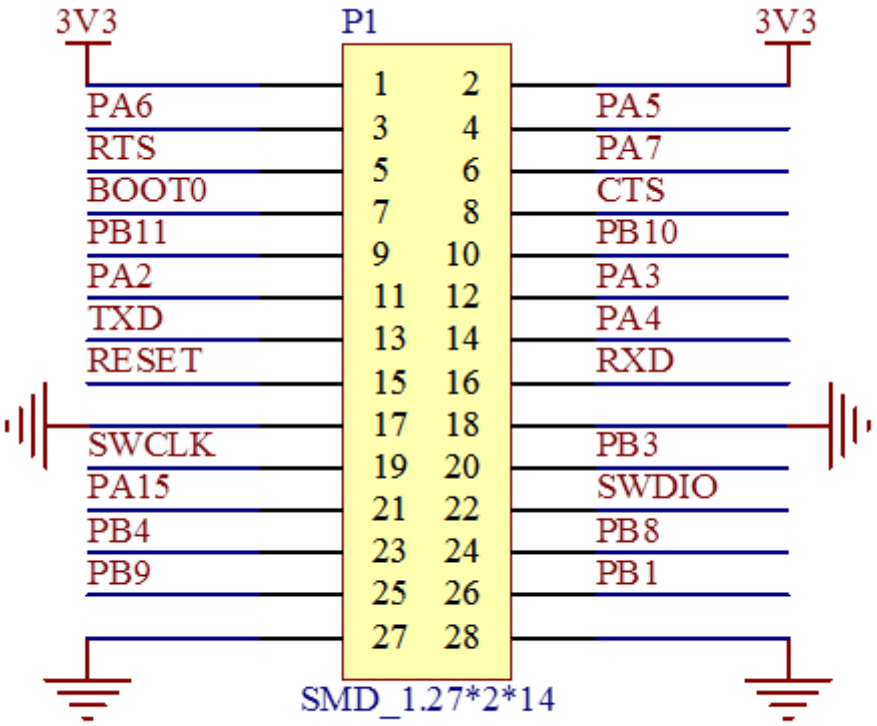
- State-of-art SI4432 chip adopted
- Embedded with 32-bit STM32F microcontroller
- Easy to integrate for hardware equipment manufacturers
- Wide communication range and high network reliability

3. Specifications

Dimensions (L*W*H)	41.00×21.50×9.95mm
Maximum Transmit Range (LOS)	2000m (with External Antenna)
Maximum Output Power	20dBm
RF Data Rate	Up to 128kbps (software selectable)
Serial Data Rate (software selectable)	1200-230400 bps
RX Sensitivity (1% packet error rate)	-110dBm
Supply Voltage	3.3V±0.3V
Operating Current(Transmit)	103mA@20dBm
Operating Current(Receive)	37mA
Operating Frequency	ISM 240-960MHz
Operating Temperature	-40 to 85℃
Antenna Interface	U.FL; Helical antenna
Interface Features	24 GPIO ports; 3 serial ports UART supported; 1 SPI and I2C supported; 7x12 bits A/D ports.

4. Pin Configurations

4.1 Pin Signal

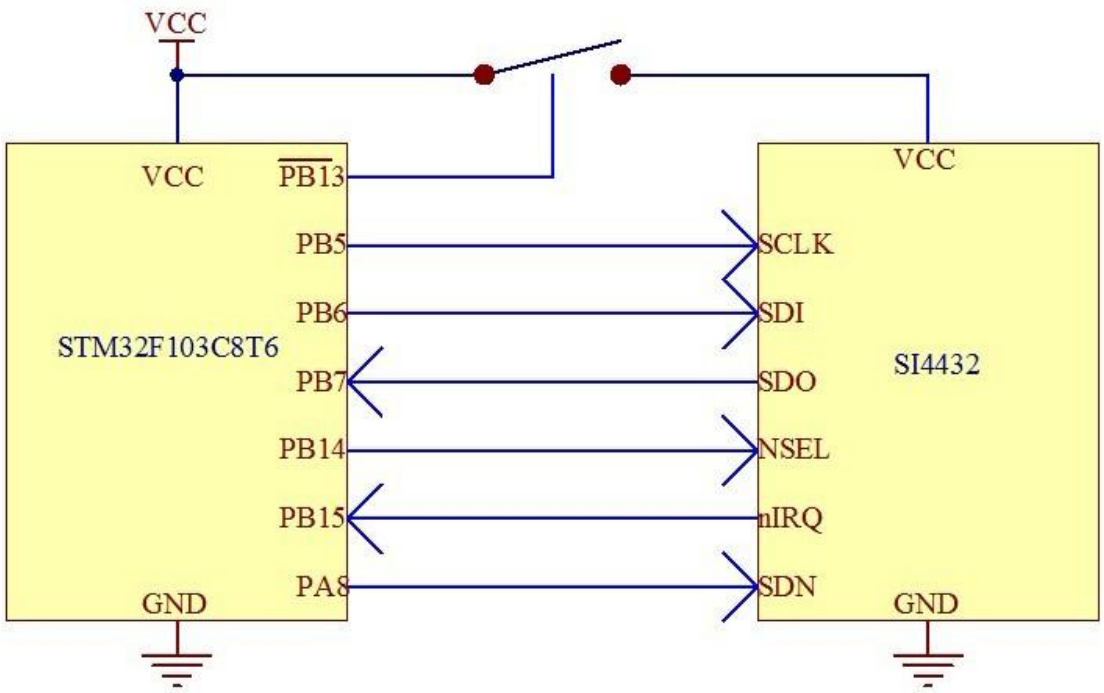


4.2 Pin Assignment

Module Pin No.	Signal	STM32F Pin No.	Default	Remap
P1-1	3V3	-	DC3.3V	
P1-2	3V3	-	DC3.3V	
P1-3	PA6	16	SPI1_MISO(8)/ADC_IN6	TIM3_CH1(8)
P1-4	PA5	15	SPI1_SCK(8)/ADC_IN5	
P1-5	RTS	33	USART1_RTS	
P1-6	PA7	17	SPI1_MOSI(8)/ADC_IN7	TIM3_CH2(8)
P1-7	BOOT0	44	-	
P1-8	CTS	32	USART1_CTS	
P1-9	PB11	22	I2C2_SDA/ USART3_RX (8)	
P1-10	PB10	21	I2C2_SCL/ USART3_TX (8)	
P1-11	PA2	12	USART2_TX(8)/ ADC_IN2/TIM2_CH3(8)	

Module Pin No.	Signal	STM32F Pin No.	Default	Remap
P1-12	PA3	13	USART2_RX(8)/ ADC_IN3/TIM2_CH4(8)	
P1-13	TXD	30	USART1_TX(8)	
P1-14	PA4	14	SPI1_NSS(8)/ADC_IN4 USART2_CK(8)/	
P1-15	NRESET	7	-	
P1-16	RXD	31	USART1_RX(8)	
P1-17	GND	-	Ground	
P1-18	GND	-	Ground	
P1-19	SWCLK	37	-	
P1-20	PB3	39	-	
P1-21	PA15	38	-	
P1-22	SWDIO	34	-	
P1-23	PB4	40	-	
P1-24	PB8	45	TIM4_CH3 I2C1_SCL/CANRX	
P1-25	PB9	46	TIM4_CH4 I2C1_SDA/CANTX	
P1-26	PB1	19	ADC_IN9/TIM3_CH4(8)	
P1-27	GND	-	Ground	
P1-28	GND	-	Ground	

5. System Block Diagram



Module firmware development:

- **Development tool: J-Link**

Download links: http://www.segger.com/jlink-software.html

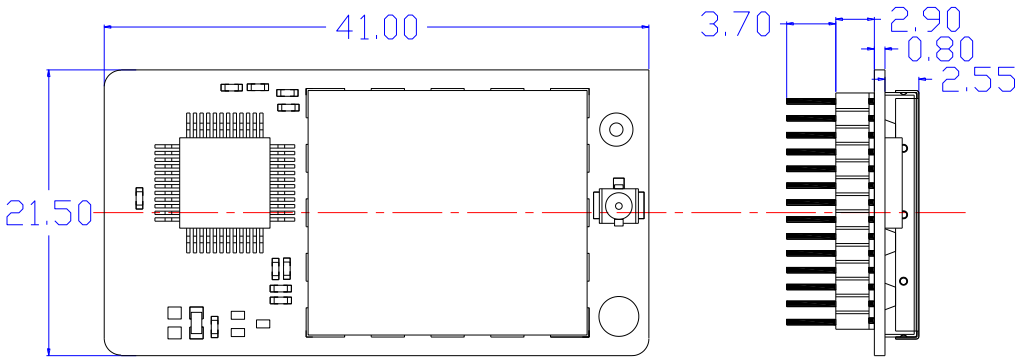
- **Integrated development environment: IAR**

Download links: http://www.iar.com/en/Products/IAR-Embedded-Workbench/ARM/

- **Development Board: Enhanced Development Board**

Download links: http://www.rexense.com/en/products_det.php?classid=34&idd=65

6. Outline Drawings



Outline Drawings (in mm)

7. Contact Us

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