REXENSE 瑞瀛

802.15.4/ZigBee Module Datasheet

REX3SP

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VERSION HISTORY

V1.0.0	2011/06/04	1st issue of preliminary document
V1.0.2	2012/09/26	3.6.2 Reference Design (Dual-Voltage) Modified
V1.0.3	2014/10/14	Default chip changed to EM357

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1. Introduction

1.1 Summary

REX3SP is an ultra-compact, low-power, high-sensitivity 2.4 GHz IEEE 802.15.4/ZigBee module based on the innovative Rexense's hardware platform. It is designed for wireless sensing, control and data acquisition applications. RexBee modules eliminate the need for costly and time-consuming RF development, and shorten time to market for a wide range of wireless applications.

1.2 Applications

RexBee module is compatible with robust IEEE 802.15.4/ZigBee stack that supports a self-healing, self-organizing mesh network, while optimizing network traffic and minimizing power consumption. Rexense offers two stack configurations: Custom and Transparent (currently supports STM32W RexBee module only). Custom software supports reliable, scalable, and secure wireless applications running on RexBee modules. Transparent software allows programming of the module via serial AT-command interface.

The applications include, but are not limited to:

- Building automation & monitoring
  - Lighting controls
  - Wireless smoke and CO detectors
  - Structural integrity monitoring
- HVAC monitoring & control
- Inventory management
- Environmental monitoring
- Security
- Water metering
- Industrial monitoring
  - Machinery condition and performance monitoring
  - Monitoring of plant system parameters such as temperature, pressure, flow, tank level, humidity, vibration, etc.
- Automated meter reading (AMR)

1.3 Key Features

- Size：31.60*20.70*3.90mm
- Output power：23dBm
- High RX sensitivity：-104dBm
- Outperforming link budget：127dB
- Wide Communication Distance: 2000m (Line of Sight)
- Very low power consumption:
  - Sleep mode：<2.0μA
  - RX mode：29mA
  - TX mode：170mA@20dBm；230mA@23dBm
- Ample memory resources:
  - EM351/EM357： 128K/192K bytes Flash；12K bytes RAM
  - STM32W：128K bytes Flash； 8K bytes RAM
- Wide range of interfaces (both analog and digital):
  - 24 spare GPIO, 4 spare IRQ lines
  - 6 x14 bit ADC lines
  - 1 x USART
  - 1 x TWI
  - 1 x SPI/I^2C
  - Capability to write own MAC address into the Flash
  - Optional antenna reference designs
  - IEEE 802.15.4 compliant transceiver
  - 2.4 GHz ISM band
  - Custom embedded software, including serial bootloader and AT command set

1.4 Advantage

- Small physical footprint and low profile for optimum fit in even the smallest of devices.
- Best-in-class RF link range
- Extended battery life
- 4 PCB board, good ESD/EMC protection ability.
- Ample memory for user software application
- Mesh networking capability
- Easy-to-use low cost Evaluation Kit
- ISM worldwide license-free operation
- FCC certified：FCC ID：O46RY12M02

1.5 Abbreviations and Acronyms

ADC	Analog-to -Digital Converter
API	Application Programming Interface
DC	Direct Current
DTR	Data Terminal Ready
DIP	Dual In-line package
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
HAL	Hardware Abstraction Layer
HVAC	Heating, Ventilating and Air Conditioning
HW	Hardware
TWI	Inter-Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IRQ	Interrupt Request
ISM	Industrial, Scientific and Medical radio band
JTAG	Digital interface for debugging of embedded device, also known as IEEE 1149.1 standard interface
MAC	Medium Access Control layer
MCU	Microcontroller Unit. In this document it also means the processor, which is the core of ZigBee module
NWK	Network layer
OEM	Original Equipment Manufacturer
OTA	Over-The-Air upgrade
PCB	Printed Circuit Board
PER	Package Error Ratio
PHY	Physical layer
RAM	Random Access Memory
RF	Radio Frequency
RTS/CTS	Request to Send/ Clear to Send
RX	Receiver
SMA	Surface Mount Assembly
SPI	Serial Peripheral Interface
SW	Software
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter

USB	Universal Serial Bus
ZDK	ZigBee Development Kit
ZigBeePRO	Wireless networking standards targeted at low-power applications
802.15.4	The IEEE 802.15.4-2003 standard applicable to low-rate wireless PAN

1.6 Related Documents

[1] IEEE Std 802.15.4-2003 IEEE Standard for Information technology - Part 15.4 Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)

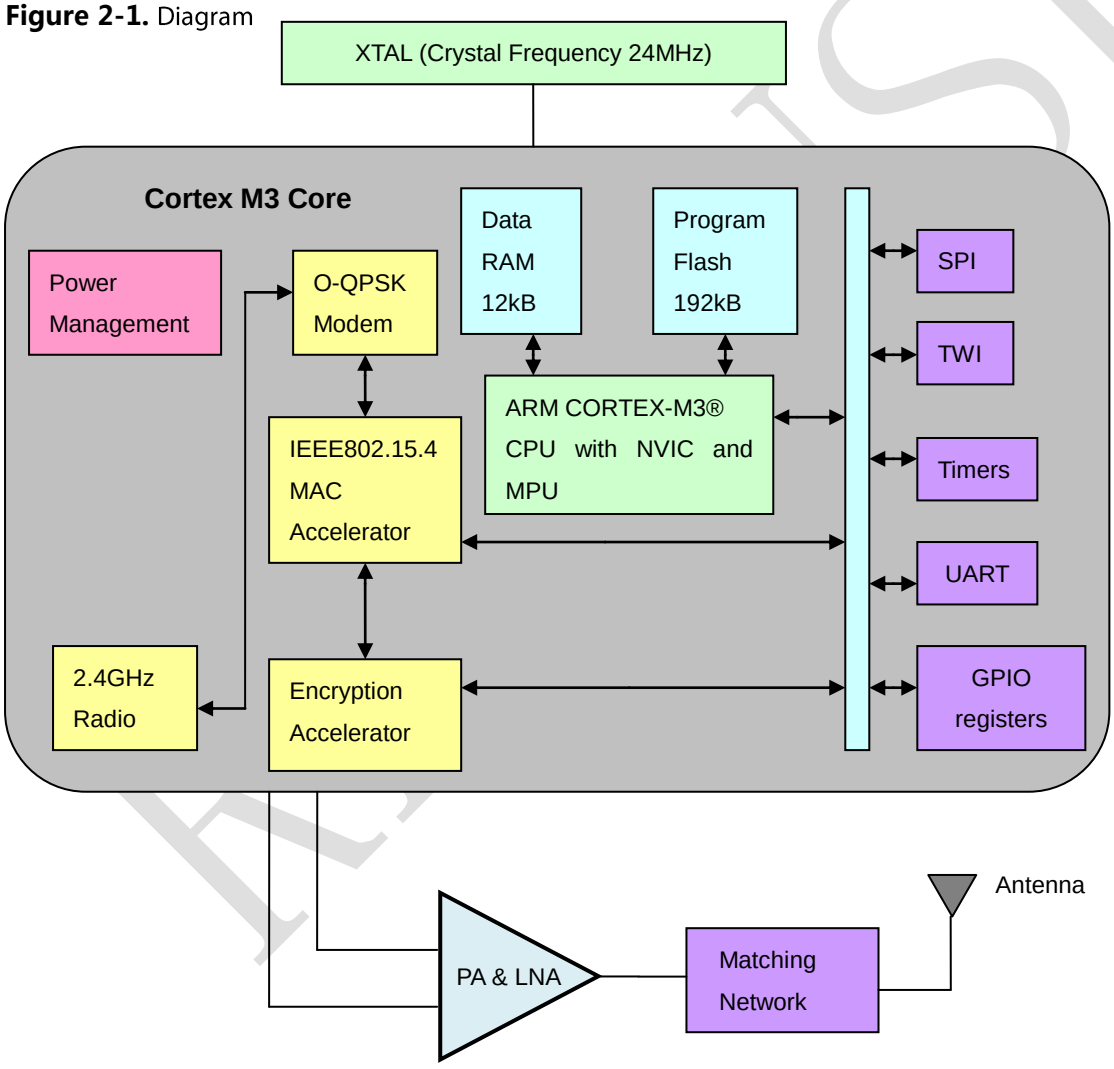
[2] ZigBee Specification. ZigBee Document 053474r17, October 19, 2007

2. Product Overview

2.1 Overview

REX3SP is a low-power, high-sensitivity IEEE 802.15.4/ ZigBee-compliant module. This multi-functional state-of-art module occupies ultra-small space, which is comparable to a typical size of a single chip. Based on a solid combination of Rexense's latest MCU Wireless hardware platform, the RexBee module offers superior radio performance, ultra-low power consumption, and exceptional ease of integration.

Figure 2-1. Diagram



REX3SP RexBee module complies with the FCC (Part 15), IC and ETSI (CE) rules applicable to the devices radiating in uncontrolled environment. REX3SP RexBee module fully satisfies the requirements of the "Directive 2002/95/EC of the European Parliament and the Council of 27January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment" (RoHS).

To jumpstart evaluation and development, Rexense also offers a complete set of evaluation and development tools. The ZigBee Development Kit comes with everything you need to develop and test your own applications.

3. Specifications

3.1. Electrical Characteristics

3.1.1. Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Parameters	Min	Max
Power supply range (VCC)	2.1V	3.6V
Pin working voltage range (except ADC pin)	-0.3V	VDD_PADS+0.3
ADC pin working voltage range	-0.3V	2.0V
Max drive current data for all I/O		40 mA
Max RX RF levle		+10 dBm

Note:

Absolute Maximum Ratings are the values beyond which damage to the module may occur.

Under no circumstances must the absolute maximum ratings given in this table be violated. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the module.

3.1.2. Test Conditions

Table 3-2. Test conditions (unless otherwise stated), VCC = 3.3V, Tamp = 25°C

Parameter	Range	Unit
Supply Voltage, VCC	2.1 to 3.6	V
RX current	29	mA
TX current (@20dBm)	170	mA
TX current (@23dBm)	230	mA
Sleeping current	<2.0	μA
TX power	-9 to +23	dBm

3.1.3. RF Characteristics

Table 3-3. RF Characteristics

Parameter	Condition	Range	Unit
Frequency Band		2400~2483.5	MHz
Numbers of Channels		16	
Channel Number		0B~1A	Hex
Channel Interval		5	MHz
Transmitter Output Power		-9 to +23	dBm
Receive Sensitivity	Packct Loss ≤1%	-104	dBm
Max data transmit speed		250	kbps
TX Output/ RX Input Nominal Impedance	For unbalanced output	50	Ω

3.1.4. Microcontroller Characteristics

Table 3-4. Microcontroller Characteristics

Parameter	Condition	Range	Unit
On-chip Flash Memory size		192KB	bytes
On-chip RAM size		12KB	bytes
Operation Frequency		24	MHz

3.1.5. Module Interfaces characteristics

Table 3-5. Module Interfaces characteristics

Parameter	Condition	Range	Unit
UART Maximum Baud Rate		230400	bps
ADC Resolution/ Conversion Time	In single conversion mode	12/4096	Bits/μs
ADC Input Resistance		>1	MΩ
ADC Reference Voltage (VREF)		1.2	V
ADC Input Voltage		0 - VREF	V
I2C Maximum Clock		400	KHz
GPIO Output Voltage (Logical 0)	-8/ 4 mA	0 ~ 0.18*VCC	V
GPIO Output Voltage (Logical 1)	-8/ 4 mA	0.82*VCC ~ VCC	V
Real Time Oscillator Frequency		32.768	KHz

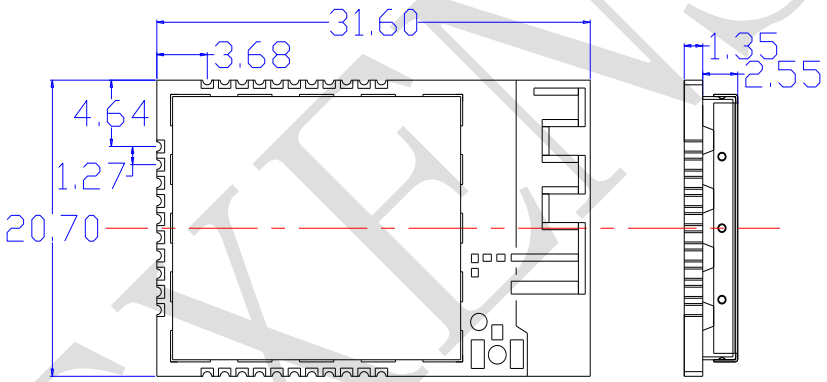
3.2. Physical/Environmental Characteristics

Table 3-6. Physical/Environmental Characteristics

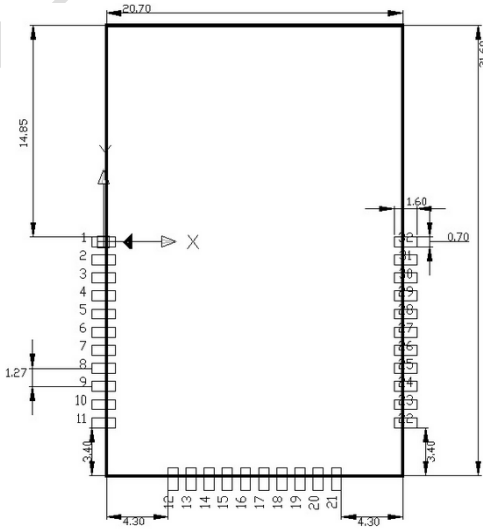
Parameter	Value	Remark
Size	31.6*20.7*3.9mm	
Weight	3.6g	
Working temp.	-40°C to +85°C	
Operating Relative Humidity Range	<95%	

3.3. Pin Configuration

Picture 3-7. Size



Picture 3-8. Package



Picture 3-9. Pin Configuration

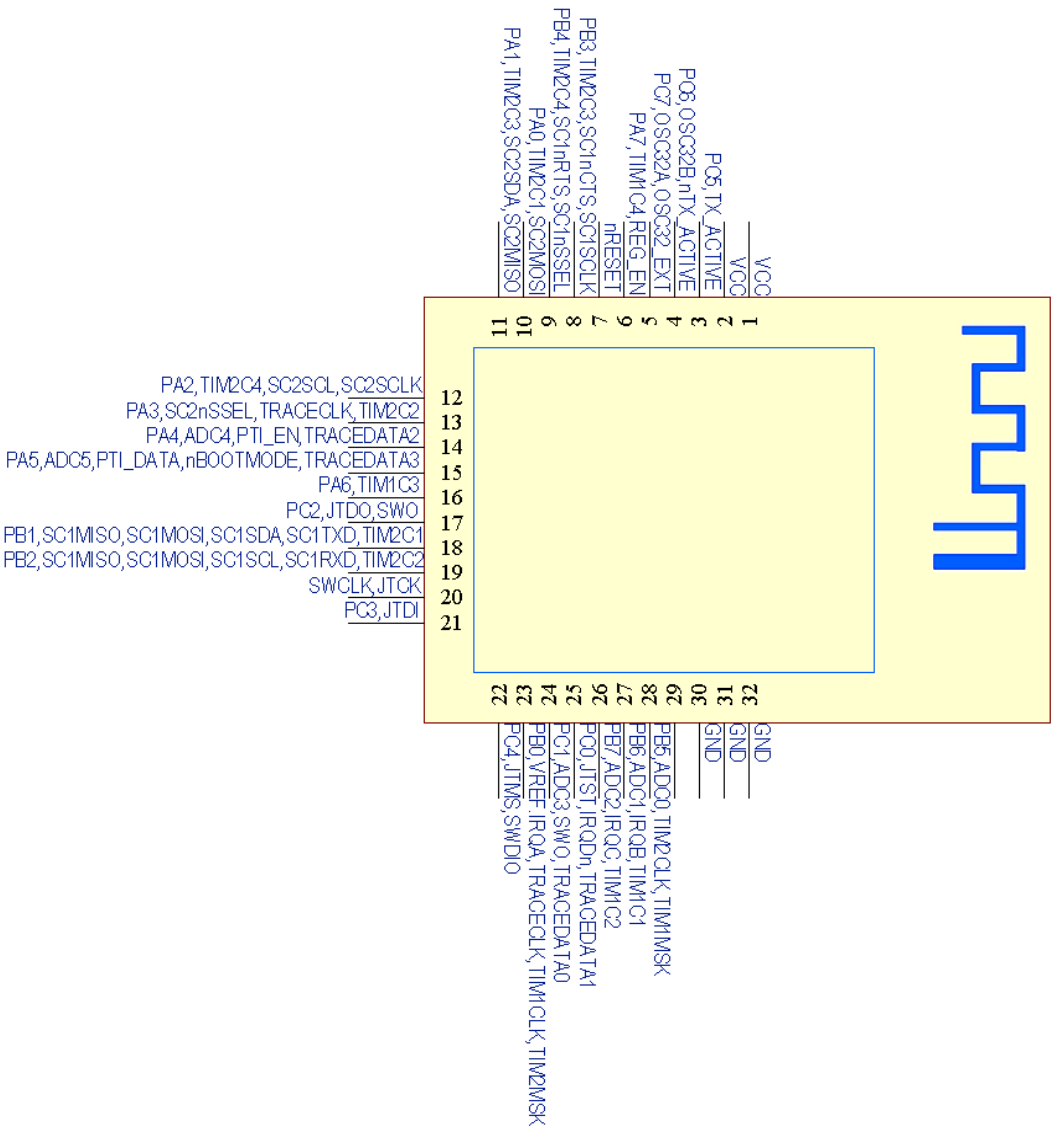


Figure 3-10. Pin instruction

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
1		3.3V	I	DC3.3V supply
2				
3	11	PC5	I/O	Digital I/O;
		TX_ACTIVE	O	Logic-level control for external Rx/Tx switch. The STM32W108 baseband controls TX_ACTIVE and drives it high (VDD_PADS) when in Tx mode. Select alternate output function with GPIO_PCCFGH[7:4]
4	13	PC6	I/O	Digital I/O;
		OSC32B	I/O	32.768 kHz crystal oscillator Select analog function with GPIO_PCCFGH[11:8]
		nTX_ACTIVE	O	Inverted TX_ACTIVE signal (see PC5) Select alternate output function with GPIO_PCCFGH[11:8]
5	14	PC7	I/O	Digital I/O
		OSC32A	I/O	32.768 kHz crystal oscillator. Select analog function with GPIO_PCCFGH[15:12]
		OSC32_EXT	I	Digital 32 kHz clock input source
6	18	PA7	I/O High current	Digital I/O. Disable REG_EN with GPIO_DBGCFG[4]
		TIM1_CH4	O	Timer 1 Channel 4 output Enable timer output with TIM1_CCER Select alternate output function with GPIO_PACFGH[15:12] Disable REG_EN with GPIO_DBGCFG[4]
			I	Timer 1 Channel 4 input. (Cannot be remapped.)
		REG_EN	O	External regulator open drain output. (Enabled after reset.)
7	12	nRESET	I	Active low chip reset (internal pull-up)
8	19	PB3	I/O	Digital I/O
		TIM2_CH3	O	Timer 2 channel 3 output Enable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGL[15:12]
			I	Timer 2 channel 3 input. Enable remap with TIM2_OR[6].
		UART_CTS	I	UART CTS handshake of Serial Controller 1 Enable with SC1_UARTCFG[5] Select UART with SC1_MODE

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		SC1SCLK	O	SPI master clock of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[6] Enable master with SC1_SPICFG[4] Select SPI with SC1_MODE Select alternate output function with GPIO_PBCFGL[15:12]
			I	SPI slave clock of Serial Controller 1 Enable slave with SC1_SPICFG[4] Select SPI with SC1_MODE
9	20	PB4	I/O	Digital I/O
		TIM2_CH4	O	Timer 2 channel 4 output Enable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGH[3:0]
			I	Timer 2 channel 4 input. Enable remap with TIM2_OR[7].
		UART_RTS	O	UART RTS handshake of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[7] Enable with SC1_UARTCFG[5] Select UART with SC1_MODE Select alternate output function with GPIO_PBCFGH[3:0]
		SC1nSSEL	I	SPI slave select of Serial Controller 1 Enable slave with SC1_SPICFG[4] Select SPI with SC1_MODE
10	21	PA0	I/O	Digital I/O
		TIM2_CH1	O	Timer 2 channel 1 output Disable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[3:0]
			I	Timer 2 channel 1 input. Disable remap with TIM2_OR[4].
		SC2MOSI	O	SPI master data out of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[4] Enable master with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[3:0]
			I	SPI slave data in of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
11	22	PA1	I/O	Digital I/O
		TIM2_CH3	O	Timer 2 channel 3 output Disable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[7:4]
			I	Timer 2 channel 3 input. Disable remap with TIM2_OR[6].
		SC2SDA	I/O	TWI data of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[6] Select TWI with SC2_MODE Select alternate open-drain output function

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
				with GPIO_PACFGL[7:4]
		SC2MISO	O	SPI slave data out of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[6] Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[7:4]
			I	SPI master data in of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
12	24	PA2	I/O	Digital I/O
		TIM2_CH4	O	Timer 2 channel 4 output Disable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[11:8]
			I	Timer 2 channel 4 input. Disable remap with TIM2_OR[7].
		SC2SCL	I/O	TWI clock of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[7] Select TWI with SC2_MODE Select alternate open-drain output function with GPIO_PACFGL[11:8]
		SC2SCLK	O	SPI master clock of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[7] Enable master with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[11:8]
			I	SPI slave clock of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
13	25	PA3	I/O	Digital I/O
		SC2nSSEL	I	SPI slave select of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
		TRACECLK	O	Synchronous CPU trace clock Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[5] Enable trace interface in ARM core Select alternate output function with GPIO_PACFGL[15:12]
		TIM2_CH2	O	Timer 2 channel 2 output Disable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[15:12]
			I	Timer 2 channel 2 input. Disable remap with TIM2_OR[5].
14	26	PA4	I/O	Digital I/O
		ADC4	Analog	ADC Input 4. Select analog function with GPIO_PACFGH[3:0].
		PTI_EN	O	Frame signal of Packet Trace Interface (PTI). Disable trace

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
				interface in ARM core. Select alternate output function with GPIO_PACFGH[3:0].
		TRACE DATA2	O	Synchronous CPU trace data bit 2. Select 4-wire synchronous trace interface in ARM core. Enable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[3:0].
15	27	PA5	I/O	Digital I/O
		ADC5	Analog	ADC Input 5. Select analog function with GPIO_PACFGH[7:4].
		PTI_DATA	O	Data signal of Packet Trace Interface (PTI). Disable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[7:4].
		nBOOT MODE	I	Embedded serial bootloader activation out of reset. Signal is active during and immediately after a reset on NRST.
		TRACE DATA3	O	Synchronous CPU trace data bit 3. Select 4-wire synchronous trace interface in ARM core. Enable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[7:4]
16	29	PA6	I/O High current	Digital I/O
		TIM1_CH3	O	Timer 1 channel 3 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PACFGH[11:8]
			I	Timer 1 channel 3 input (Cannot be remapped.)
17	33	PC2	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
		JTDO	O	JTAG data out to debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35)
		SWO	O	Serial Wire Output asynchronous trace output to debugger Select asynchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[11:8] Enable Serial Wire mode (see JTMS description, Pin 35) Internal pull-up is enabled
18	30	PB1	I/O	Digital I/O
		SC1MISO	O	SPI slave data out of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select SPI with SC1_MODE Select slave with SC1_SPICR Select alternate output function with GPIO_PBCFGL[7:4]
		SC1MOSI	O	SPI master data out of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select SPI with SC1_MODE Select master with

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
				SC1_SPICR Select alternate output function with GPIO_PBCFGL[7:4]
		SC1SDA	I/O	TWI data of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4] Select TWI with SC1_MODE Select alternate open-drain output function with GPIO_PBCFGL[7:4]
		SC1TXD	O	UART transmit data of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select UART with SC1_MODE Select alternate output function with GPIO_PBCFGL[7:4]
		TIM2_CH1	O	Timer 2 channel 1 output Enable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[7:4]
			I	Timer 2 channel 1 input. Disable remap with TIM2_OR[4].
19	31	PB2	I/O	Digital I/O
		SC1MISO	I	SPI master data in of Serial Controller 1 Select SPI with SC1_MODE Select master with SC1_SPICR
		SC1MOSI	I	SPI slave data in of Serial Controller 1 Select SPI with SC1_MODE Select slave with SC1_SPICR
		SC1SCL	I/O	TWI clock of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[5] Select TWI with SC1_MODE Select alternate open-drain output function with GPIO_PBCFGL[11:8]
		SC1RXD	I	UART receive data of Serial Controller 1 Select UART with SC1_MODE
		TIM2_CH2	O	Timer 2 channel 2 output Enable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGL[11:8]
			I	Timer 2 channel 2 input. Enable remap with TIM2_OR[5].
20	32	SWCLK	I/O	Serial Wire clock input/output with debugger Selected when in Serial Wire mode (see JTMS description, Pin 35)
		JTCK	I	JTAG clock input from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35) Internal pull-down is enabled
21	34	PC3	I/O	Digital I/O Either Enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description)
		JTDI	I	JTAG data in from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35) Internal pull-up is enabled

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
22	35	PC4	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
		JTMS	I	JTAG mode select from debugger Selected when in JTAG mode (default mode) JTAG mode is enabled after power-up or by forcing NRST low Select Serial Wire mode using the ARM-defined protocol through a debugger Internal pull-up is enabled
		SWDIO	I/O	Serial Wire bidirectional data to/from debugger Enable Serial Wire mode (see JTMS description) Select Serial Wire mode using the ARM-defined protocol through a debugger Internal pull-up is enabled
23	36	PB0	I/O	Digital I/O
		VREF	Analog O	ADC reference output. Enable analog function with GPIO_PBCFGL[3:0].
		VREF	Analog I	ADC reference input. Enable analog function with GPIO_PBCFGL[3:0]. Enable reference output with an ST system function.
		IRQA	I	External interrupt source A.
		TRACECLK	O	Synchronous CPU trace clock. Enable trace interface in ARM core. Select alternate output function with GPIO_PBCFGL[3:0].
		TIM1CLK	I	Timer 1 external clock input.
		TIM2MSK	I	Timer 2 external clock mask input.
24	38	PC1	I/O	Digital I/O
		ADC3	Analog	ADC Input 3 Enable analog function with GPIO_PCCFGL[7:4]
		SWO	O	Serial Wire Output asynchronous trace output to debugger Select asynchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[7:4]
		TRACEDATA0	O	Synchronous CPU trace data bit 0 Select 1-, 2- or 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[7:4]
25	40	PC0	I/O High current	Digital I/O Either enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pin 35) and disable TRACEDATA1
		JRST	I	JTAG reset input from debugger Selected when in JTAG mode (default mode, see JTMS description) and TRACEDATA1 is

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
				disabled Internal pull-up is enabled
		IRQD (1)	I	Default external interrupt source D
		TRACE DATA1	O	Synchronous CPU trace data bit 1 Select 2- or 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[3:0]
26	41	PB7	I/O High current	Digital I/O
		ADC2	Analog	ADC Input 2 Enable analog function with GPIO_PBCFGH[15:12]
		IRQC (1)	I	Default external interrupt source C
		TIM1_CH2	O	Timer 1 channel 2 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PBCFGH[15:12]
			I	Timer 1 channel 2 input (Cannot be remapped)
27	42	PB6	I/O High current	Digital I/O
		ADC1	Analog	ADC Input 1 Enable analog function with GPIO_PBCFGH[11:8]
		IRQB	I	External interrupt source B
		TIM1_CH1	O	Timer 1 channel 1 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PBCFGH[11:8]
			I	Timer 1 channel 1 input (Cannot be remapped)
28	43	PB5	I/O	Digital I/O
		ADC0	Analog	ADC Input 0 Enable analog function with GPIO_PBCFGH[7:4]
		TIM2CLK	I	Timer 2 external clock input
		TIM1MSK	I	Timer 2 external clock mask input
29		NC	-	No connect
30		GND	-	Ground
31				
32				

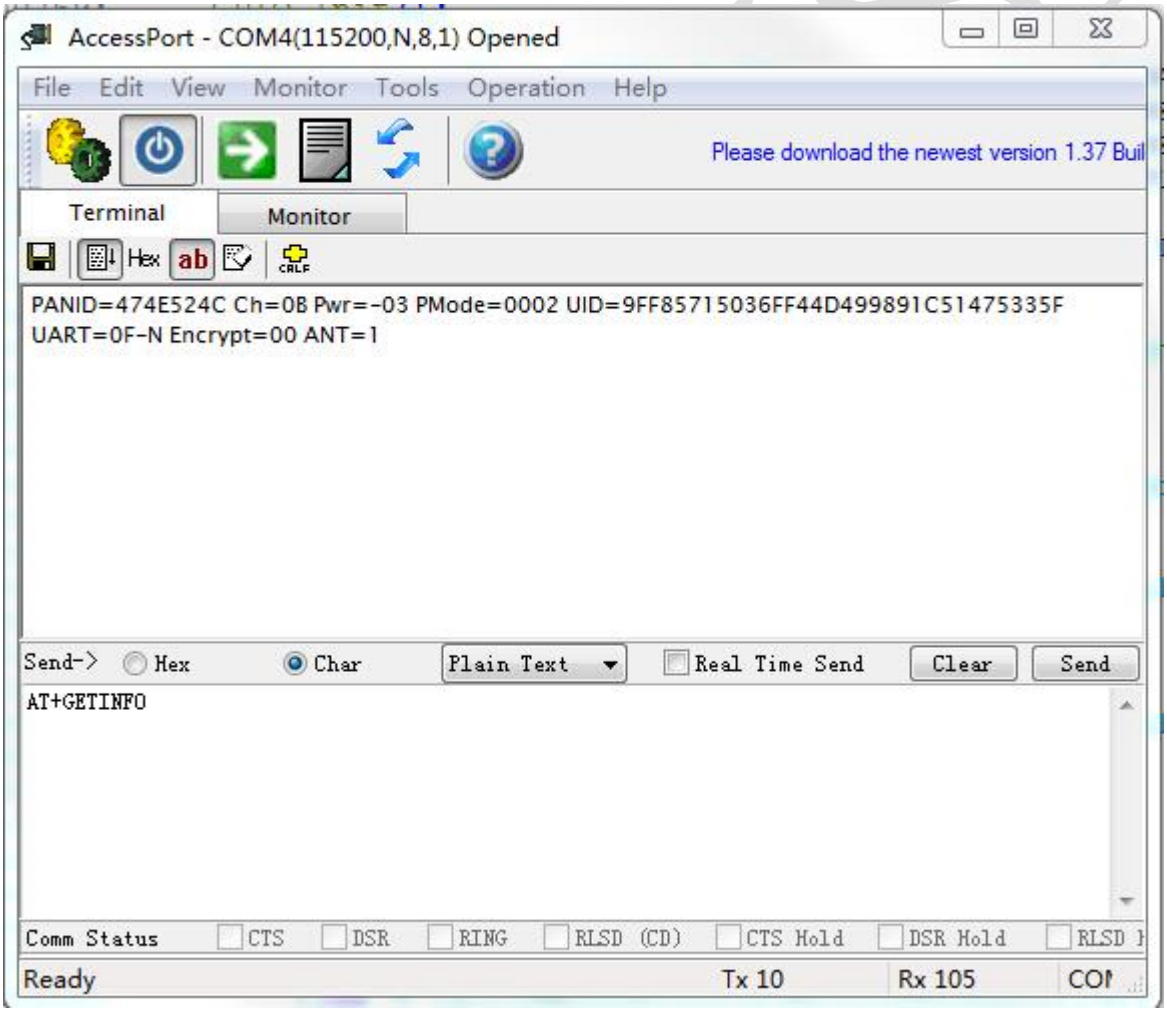
3.4. Power Mode Configuration

This part helps users to configure the power mode of RexBee module (currently only supports STM32W RexBee Module) through UART.

Users can refer to our AT commands manual to complete the UART configuration through serial port debugging software (such as AccessPort). The default UART baud rate of COO and HHU is set as 115200-8-N-1; Router set as 9600-8-N-1. The normal function of UART communication can be checked with command "AT+VER". For more detailed AT commands, please refer to www.rexense.com .

Acquire the current configuration information

Users can acquire the current configuration information of the module before UART debugging with command 'AT+GETINFO'.



The return data includes basic configuration info of module :

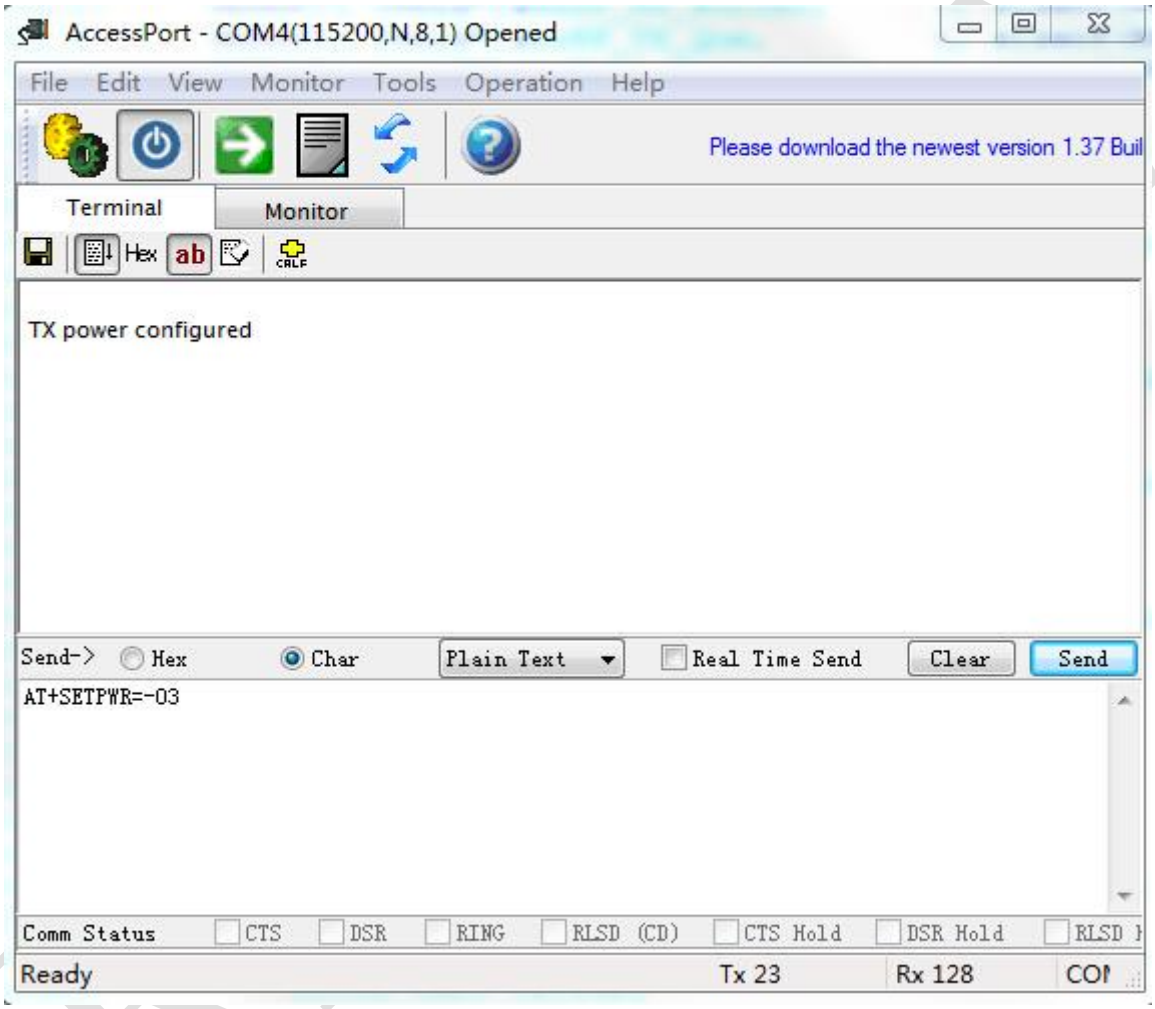
Pwr=-03 : means TX is -03dBm ;

PMode=0002 : means power mode is extra PA.

Important Note：

1. **For Enhanced RexBee module**, the TX power of the wireless chip means the TX power of the module.

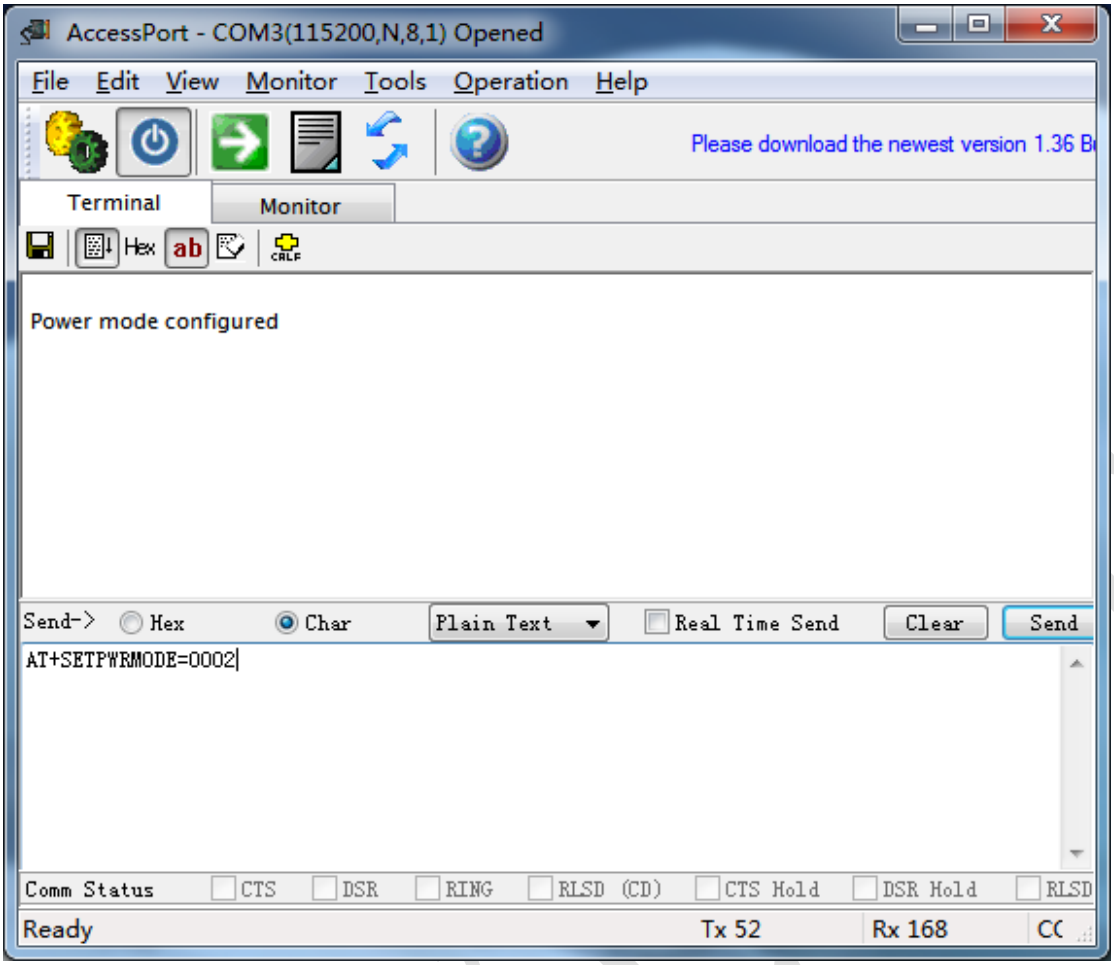
- It is recommended that the TX power set as -3dBm or -5dBm to have better communication performance.
- The TX power of the wireless chip can be configured with the command "AT+ SETPWR".



2. **For enhanced RexBee module,** the TX power of the wireless chip amplified by the power amplifier (PA) means the TX power of the module。

- Enhanced RexBee module works in **enhanced power mode** configured by the command below：

AT+SETPWRMODE=0002

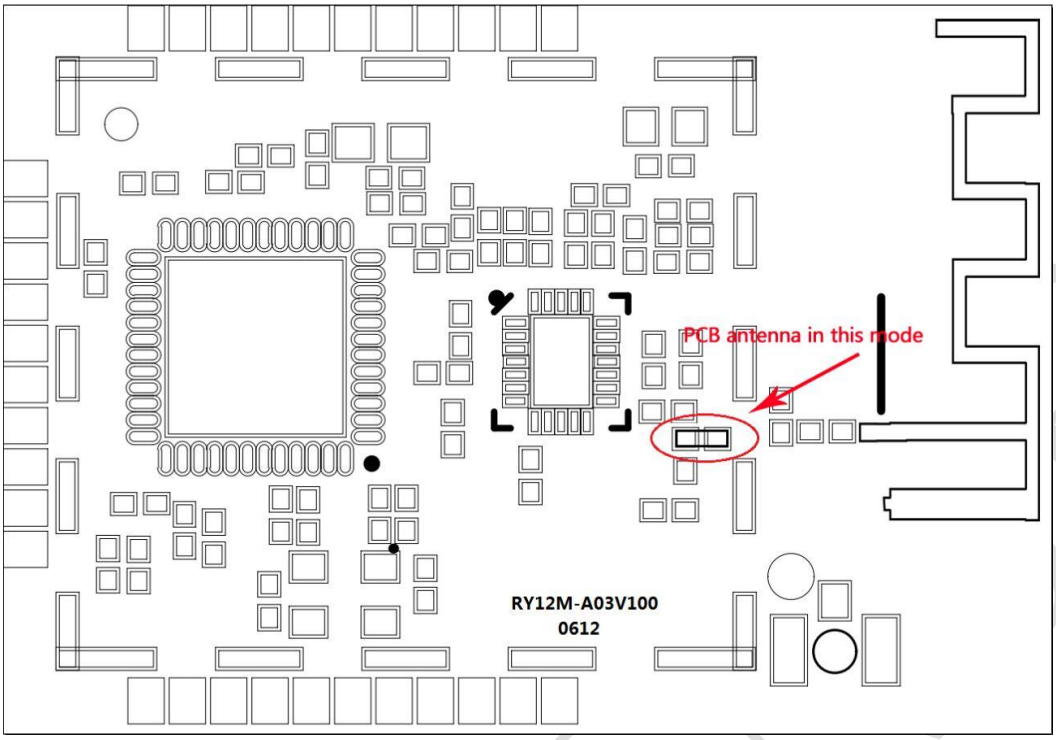


3.5 Antenna Specifications

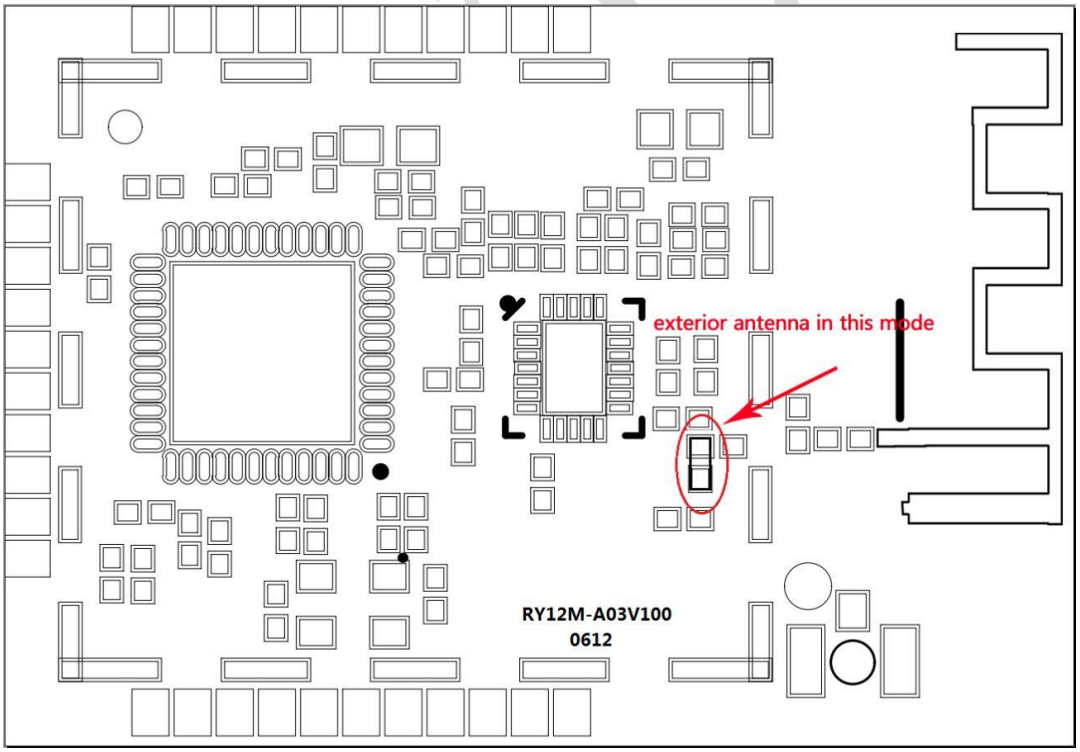
REX3SP has 4 antennas, buyer need to confirm with sales about the type before purchasing.

Figure 3-11. Jumper indication

Use PCB antenna：



Use other 3 exterior antenna：



3.5.1 PCB antenna

Figure 3-12. PCB antenna

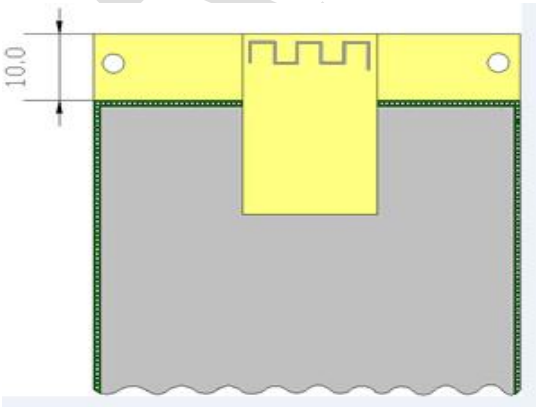
Attention when using PCB antenna：

1. Please avoid installing the module in a complete metal enclosure.
2. Please avoid placing high profile components next to antenna （1 cm at least, suggest more than 2.7 cm）
3. ZigBee module should not be placed next to consumer electronics which might interfere with ZigBee's RF frequency band.

User should try to avoid other components or line interfere PCB antenna when designing board：

- Wires or other components avoid surrounding PCB antenna
- PCB antenna should be extended to the board
- Don’t use metal shell to cover the PCB antenna

Figure 3-13. PCB Layout of the Proposed Antenna Selection

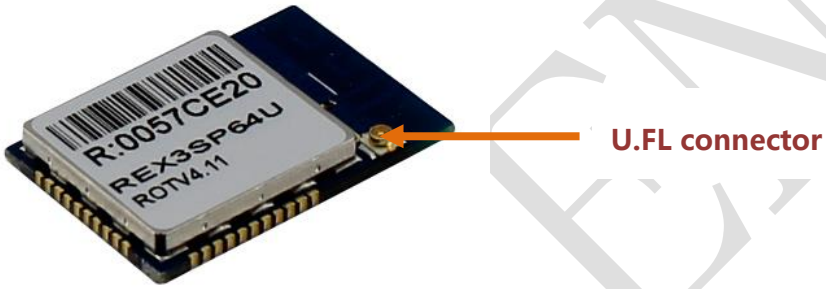


3.5.2 Steel Antenna

Figure 3-14. Steel Antenna

3.5.3 U.FL connects SMA antenna

Figure 3-15. U.FL connector



Remark：Note: when the U.FL (IPEX) connector is used, it's necessary to use the antenna cable and the SMA antenna at the same time. Please see the pictures below.

Figure 3-16. antenna cable

Figure 3-17. SMA antenna

Figure 3-18. completing picture of SMA antenna

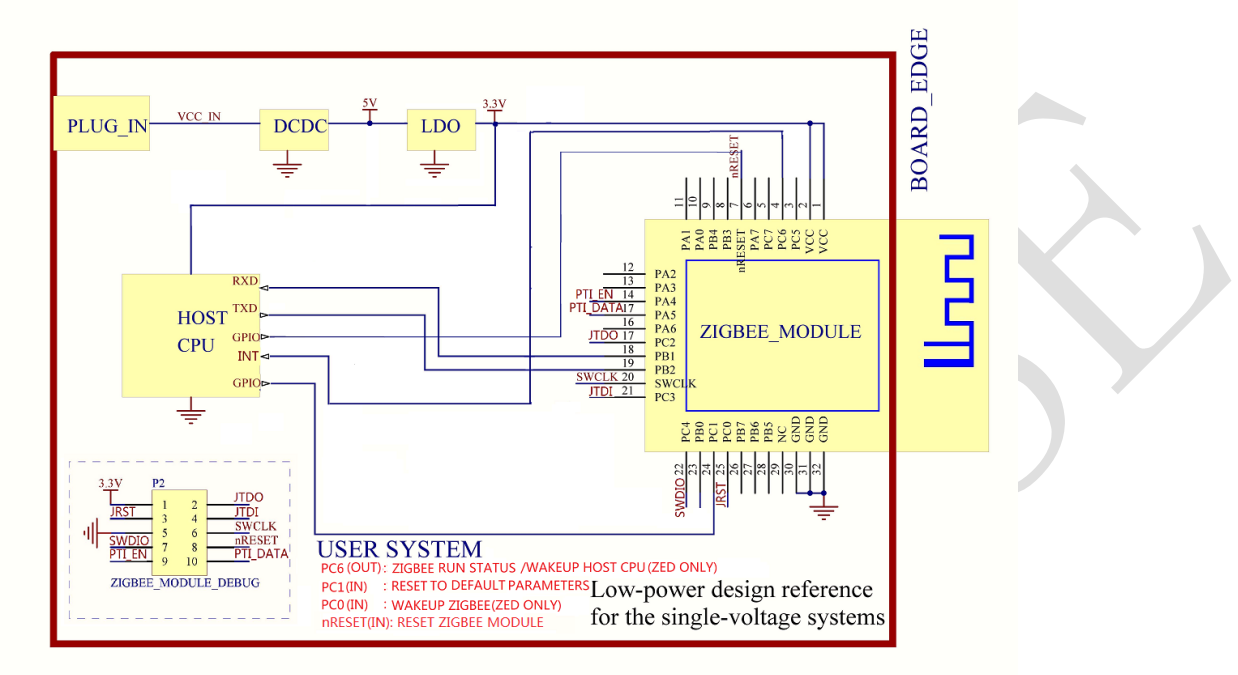
3.5.4 U.FL connects PCB antenna

Figure 3-19. connect PCB antenna

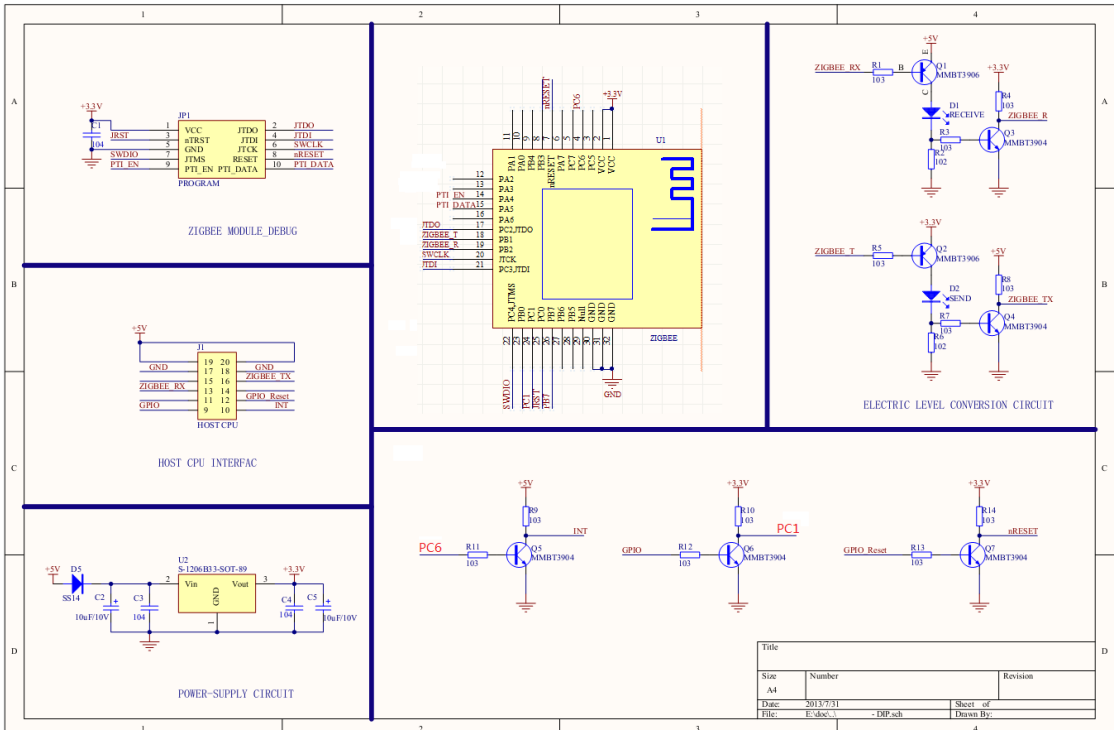
Figure 3-20. completing picture

3.6. Module Circuit Reference Design

3.6.1. When system voltage is 3.3V



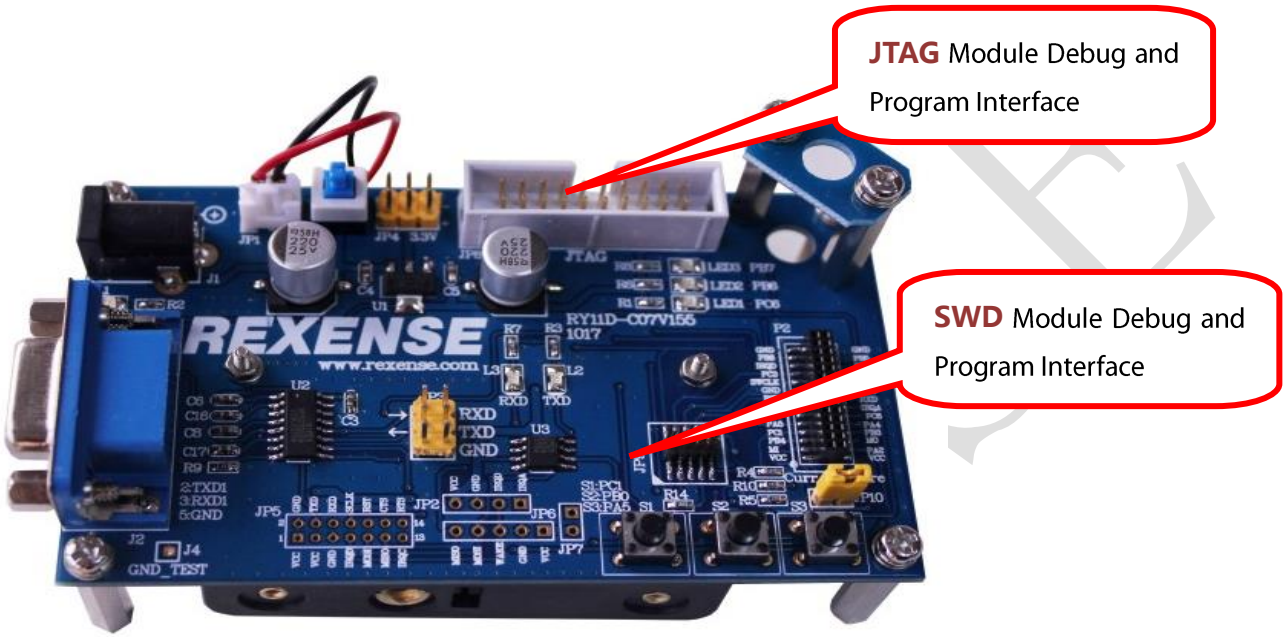
3.6.2. When system voltage is 5.0V



3.7. Module Test Instructions

3.7.1. Module Debugging

Figure 3-21. Module Debug and Program Interface



Module Debug and Program Interface as above, it doesn't' support standard JTAG connection, we suggest following SWD connection.

3.7.2. Module Debug and Program Interface connection

Figure 3-22. SWD connection

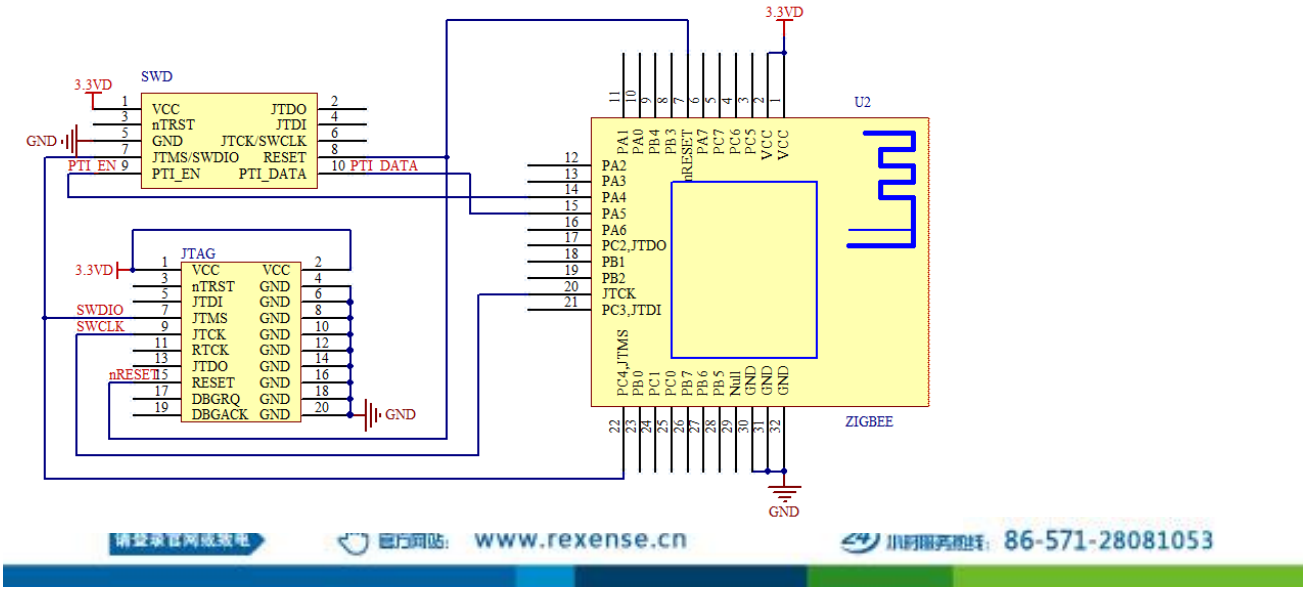


Figure 3-23. Relationship between JTAG and Module Debug and Program Interface

Zigbee module Pin NO.	20-pin JTAG Interface Pin Number (Name)	SWD connecting way and pin No. (Name)
1、2(VCC)	1(VCC)	1(VCC)
	2(VCC)	——
	3(nTRST)	——
	4(GND)	——
	5(JTDI)	——
30、31、32 (GND)	6(GND)	5(GND)
22 (PC4)	7(JTMS)	7(SWDIO)
	8(GND)	——
20 (SWCLK)	9(JTCK)	6(SWCLK)
	10(GND)	——
	11(RTCK)	——
	12(GND)	——
	13(JTDO)	——
	14(GND)	——
7 (nRESET)	15(RESET)	8(RESET)
	16(GND)	——
	17(DBGRQ)	——
	18(GND)	——
	19(DBGACK)	——
	20(GND)	——
14 (PA4)	——	9(PTI_EN)
15 (PA5)	——	10(PTI_DATA)

3.8. Test Result of RF Performance

Figure 3-24. RX sensitivity

Figure 3-25. Carrier Signal Testing

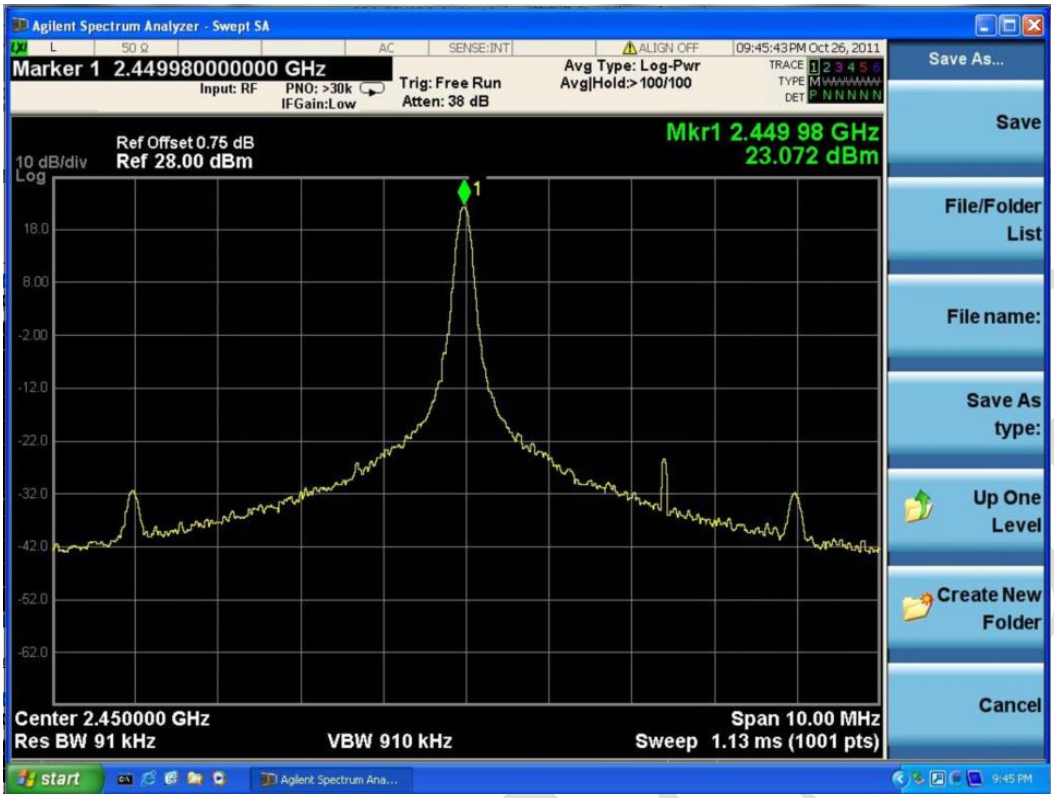


Figure 3-26. Modulating Signal Testing

4. Ordering Information

REX 3 D 57 U

Manufacturer

REX=REXENSE

Serial

3=Zigbee serial (Cortex™-M3 Core)

Package type

D=DIP

S=SMD

U=Ultra compact

L=LED lighting

Chip No.

51=EM351

57=EM357 (default)

64=STM32W108CBU64

Antenna

U=U.FL connector (default)

B=PCB antenna

L=L antenna

P=Pin out

S=SMA antenna

H=Spring antenna

5. Contact Us

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