REXENSE 瑞瀛

802.15.4/ZigBee Module Datasheet

REX3U

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VERSION HISTORY

V1.0.0	2014/07/21	1st issue of preliminary document
V1.0.2	2014/08/21	Revised version
V1.0.3	2014/11/17	Revised for Ember357 version

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Contents

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1. Introduction

1.1 Summary

REX3U is an ultra-compact, low-power, high-sensitivity 2.4 GHz IEEE 802.15.4/ZigBee module based on the innovative Rexense's hardware platform. It is designed for wireless sensing, control and data acquisition applications. And this module has a specialized firmware for LED lights, support grouping, timing, scene mode, wireless updating for firmware, parameter setting. RexBee modules eliminate the need for costly and time-consuming RF development, and shorten time to market for a wide range of wireless applications.

1.2 Applications

RexBee module is compatible with robust IEEE 802.15.4/ZigBee stack that supports a self-healing, self-organizing mesh network, while optimizing network traffic and minimizing power consumption. Rexense offers two stack configurations: Custom and Transparent. Custom software can be provided to support reliable, scalable, and secure wireless applications running on RexBee modules. Transparent software allows programming of the module via serial AT-command interface.
The applications include, but are not limited to:

- Building automation & monitoring
  - Lighting controls, ZLL, Zigbee light link
  - Wireless smoke and CO detectors
  - Structural integrity monitoring
- HVAC monitoring & control
- Inventory management
- Environmental monitoring
- Security
- Water metering
- Industrial monitoring
  - Machinery condition and performance monitoring
  - Monitoring of plant system parameters such as temperature, pressure, flow, tank level, humidity, vibration, etc.
- Automated meter reading (AMR)

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- LED light control

1.3 Key Features

- Size：18.00*15.00*2.60mm
- Output power 8dBm
- High RX sensitivity：-99 dBm
- Outperforming link budget：107dB
- Wide Communication Distance: 300m (可视距离)
- Very low power consumption
  - Sleep mode：<2.0μA
  - RX mode：29mA
  - TX mode：36mA@3dBm; 45mA@8dBm
- Ample memory resources:
  - EM357-i： 192K bytes Flash；12K bytes RAM
- Wide range of interfaces (both analog and digital):
  - 24 x GPIO，4 x interrupt source
  - 6 x 14 bit ADC channel
  - 1 x USART
  - 1 x TWI
  - 1 x SPI/I^2C
  - Capability to write own MAC address into the Flash
  - Optional antenna reference designs
  - IEEE 802.15.4 compliant transceiver
  - 2.4 GHz ISM band
  - Custom embedded software, including serial bootloader and AT command set

1.4 Advantage

- Small physical footprint and low profile for optimum fit in even the smallest of devices.
- Best-in-class RF link range
- Extended battery life
- 4 PCB board, good ESD/EMC protection ability.
- Ample memory for user software application
- Mesh networking capability

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- Easy-to-use low cost Evaluation Kit
- ISM worldwide license-free operation
- FCC certified：FCC ID：O46RY12M01

1.5 Abbreviations and Acronyms

ADC	Analog-to -Digital Converter
API	Application Programming Interface
DC	Direct Current
DTR	Data Terminal Ready
DIP	Dual In-line package
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
HAL	Hardware Abstraction Layer
HVAC	Heating, Ventilating and Air Conditioning
HW	Hardware
TWI	Inter-Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IRQ	Interrupt Request
ISM	Industrial, Scientific and Medical radio band
JTAG	Digital interface for debugging of embedded device, also known as IEEE 1149.1 standard interface
MAC	Medium Access Control layer
MCU	Microcontroller Unit. In this document it also means the processor, which is the core of ZigBee module
NWK	Network layer
OEM	Original Equipment Manufacturer
OTA	Over-The-Air upgrade
PCB	Printed Circuit Board
PER	Package Error Ratio
PHY	Physical layer
RAM	Random Access Memory
RF	Radio Frequency
RTS/CTS	Request to Send/ Clear to Send
RX	Receiver
SMA	Surface Mount Assembly
SPI	Serial Peripheral Interface

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SW	Software
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
ZDK	ZigBee Development Kit
ZigBeePRO	Wireless networking standards targeted at low-power applications
802.15.4	The IEEE 802.15.4-2003 standard applicable to low-rate wireless PAN

1.6 Related Documents

[1] IEEE Std 802.15.4-2003 IEEE Standard for Information technology - Part 15.4 Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)

[2] ZigBee Specification. ZigBee Document 053474r17, October 19, 2007

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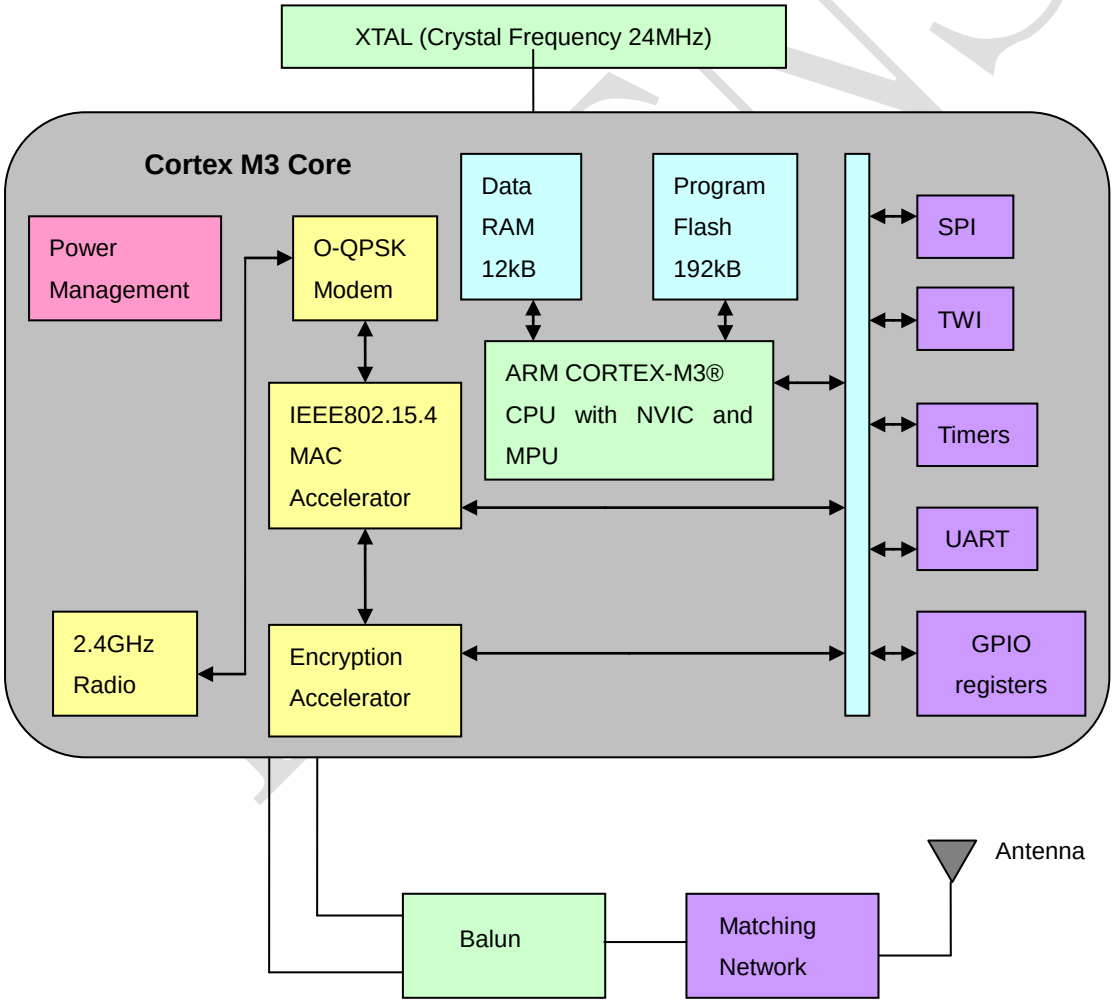
2. Product Overview

2.1 Overview

REX3U is a low-power, high-sensitivity IEEE 802.15.4/ ZigBee-compliant module. This multi-functional state-of-art module occupies ultra-small space, which is comparable to a typical size of a single chip. Based on a solid combination of Rexense's latest MCU Wireless hardware platform, RexBee module offers superior radio performance, ultra-low power consumption, and exceptional ease of integration.

Figure 2-1. Product diagram



REX3U RexBee module complies with the FCC (Part 15), IC and ETSI (CE) rules applicable to the devices radiating in uncontrolled environment.

REX3U RexBee module fully satisfies the requirements of the “Directive 2002/95/EC of the European Parliament and the Council of 27January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment” (RoHS).

To jumpstart evaluation and development, Rexense also offers a complete set of evaluation and development tools. The ZigBee Development Kit comes with everything you need to develop and test your own applications.

3. Specifications

3.1. Electrical Characteristics

3.1.1. Maximum Sustain Index

Table 3-1. Absolute Maximum Ratings

Parameters	MIN	MAX
Power supply voltage range (VCC)	2.1V	3.6V
Pin working voltage range (Except ADC)	-0.3V	VCC+0.3V
ADC pin working voltage range	-0.3V	2.0V
Max driving circuit data of all I/O on chips		40 mA
Maximum RX level		+15 dBm

Note:

Absolute Maximum Ratings are the values beyond which damage to the module may occur.

3.1.2. Testing condition

Table 3-2. testing condition (unless otherwise stated), VCC = 3.3V, Temp = 25°C

Parameter	Range	Unit
Supply Voltage, VCC	2.1 to 3.6	V
Current Consumption: RX mode	29	mA
Current Consumption: TX mode (@3dBm)	36	mA
Current Consumption: TX mode (@8dBm)	45	mA
Sleeping current	<2.0	μA

Transmitting power	-32 to +8	dBm

3.1.3. RF Characteristic

Table 3-3. RF characteristic

Parameter	Testing Condition	Range	Unit
Frequency Band		2400~2483.5	MHz
Numbers of frequency band		16	
Channel Number		0B~1A	Hex
Channel Spacing		5	MHz
Transmitter Power		-32 to +8	dBm
Receiver Sensitivity	Loss rate ≤1%	-99	dBm
Maximum transmission speed		250	kbps
Nominal Impedance of RX and TX	For unbalanced output	50	Ω

3.1.4. Microcontroller Characteristics

Table 3-4. Microcontroller Characteristics

Parameter	Condition	Range	Unit
On-chip Flash Memory size		192K	bytes
On-chip RAM size		12K	bytes
Operation Frequency		24	MHz

3.1.5. Module Interfaces characteristics

Table 3-5. Module Interfaces characteristics

Parameter	Condition	Range	Unit
UART Maximum Baud Rate		230400	bps
ADC Resolution/ Conversion Time	Half-duplex mode	12/4096	Bits/μs
ADC Input Resistance		>1	MΩ
ADC Reference Voltage (VREF)		1.2	V
ADC Input Voltage		0 - VREF	V
I2C Maximum Clock		400	kHz
GPIO Output Voltage (Logic 0)	-8/ 4 mA	0 ~ 0.18*VCC	V
GPIO Output Voltage (Logic 1)	-8/ 4 mA	0.82*VCC ~ VCC	V

Real time clock frequency		32.768	kHz

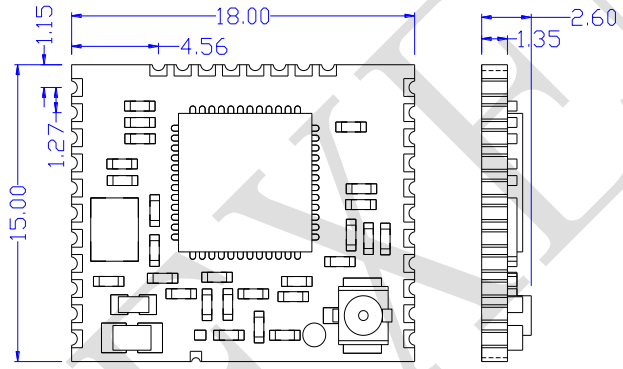
3.2. Physical/Environmental Characteristics

Table 3-6. Physical/Environmental Characteristics

Parameter	Value	Remark
Size	18.0*15.0*2.6mm	
Weithgt	1.1g	
Operating Temperature Range	-40°C to +85°C	
Operating Relative Humidity Range	<95%	

3.3. Pin Configuration

Picture3-7. External dimension drawing (mm)



Picture3-8. Packaging(mm)

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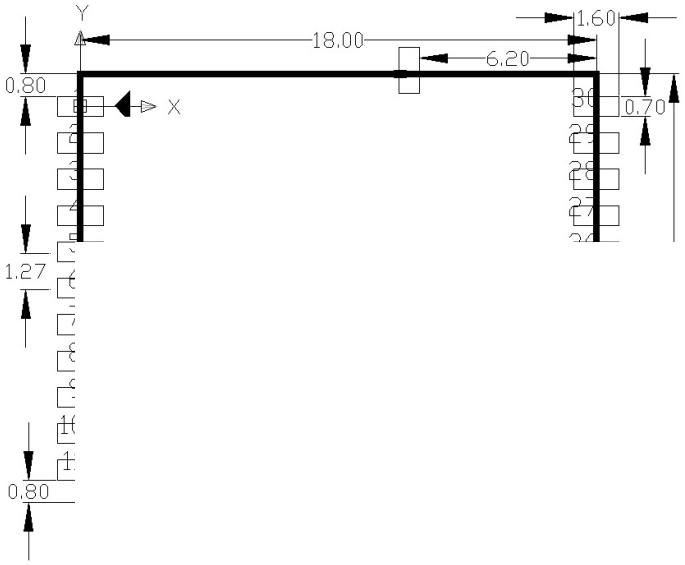
Y
X
18.00
6.20
1.60
0.70
0.80
1.27
0.80

Pictu

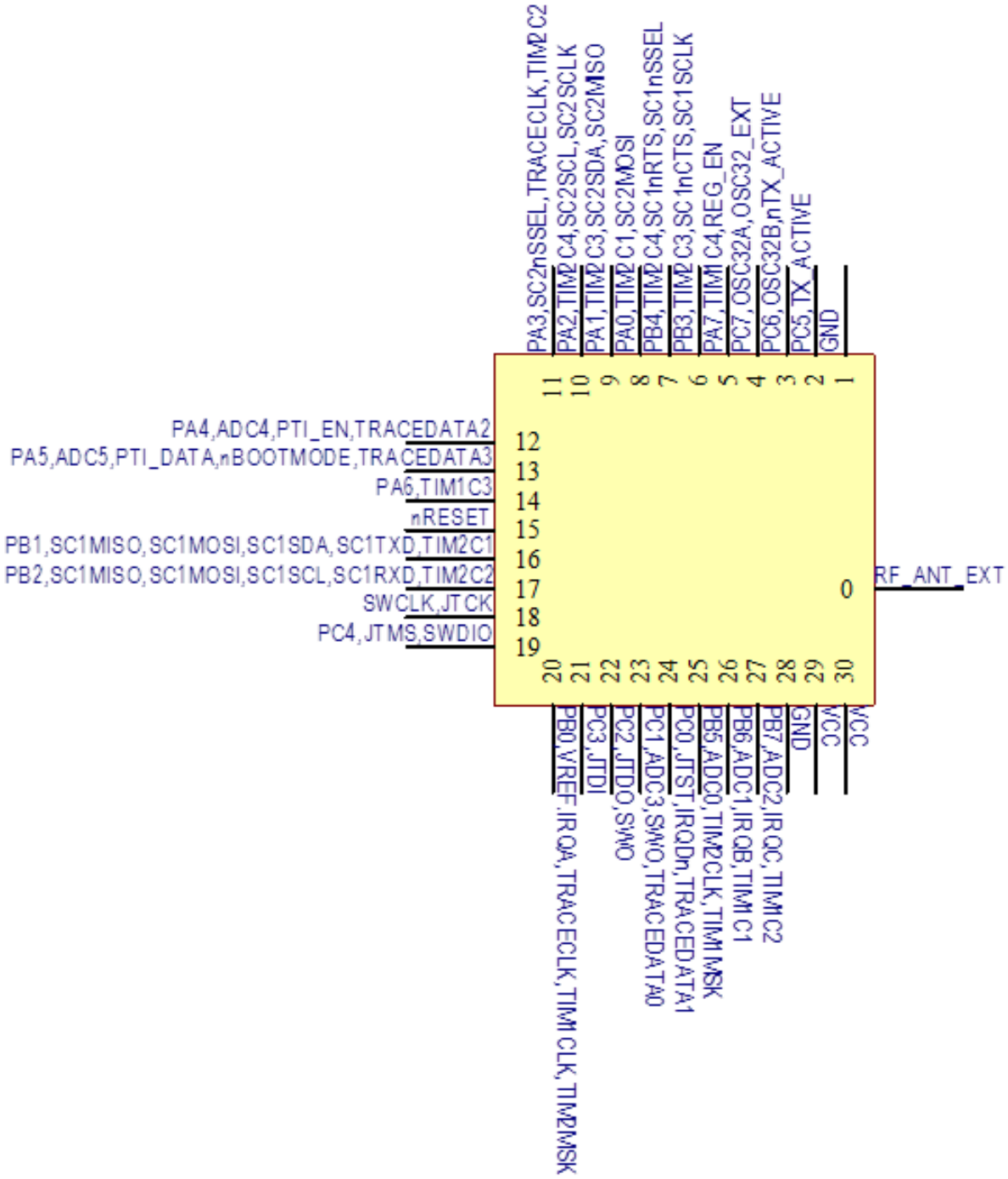
PA3,SC2nSSEL,TRACECLK,TIM2C2
PA2,TIM2C4,SC2SCL,SC2SCLK
PA1,TIM2C3,SC2SDA,SC2MISO
PA0,TIM2C1,SC2MOSI
PB4,TIM2C4,SC1nRTS,SC1nSSEL
PB3,TIM2C3,SC1nCTS,SC1SCLK
PA7,TIM1C4,REG_EN
PC7,OSC32A,OSC32_EXT
PC6,OSC32B,nTX_ACTIVE
PC5,TX_ACTIVE
GND
PA4,ADC4,PTI_EN,TRACEDATA2
PA5,ADC5,PTI_DATA,nBOOTMODE,TRACEDATA3
PA6,TIM1C3
nRESET
PB1,SC1MISO,SC1MOSI,SC1SDA,SC1TXD,TIM2C1
PB2,SC1MISO,SC1MOSI,SC1SCL,SC1RXD,TIM2C2
SWCLK,JTCK
PC4,JTMS,SWDIO
0
RF_ANT_EXT
PB0,VREF,IRQA,TRACECLK,TIM1CLK,TIM2MSK
PC3,JTDI
PC2,JTDO,SWO
PC1,ADC3,SWO,TRACEDATA0
PC0,JTST,IRQDn,TRACEDATA1
PB5,ADC0,TIM2CLK,TIM1MSK
PB6,ADC1,IRQB,TIM1C1
PB7,ADC2,IRQC,TIM1C2
GND
VCC
VCC

Table 3-10. Pin descriptions

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
1		GND	-	Ground
2	11	PC5	I/O	Digital I/O;
		TX_ACTIVE	O	Logic-level control for external Rx/Tx switch. The STM32W108 baseband controls TX_ACTIVE and drives it high (VDD_PADS) when in Tx mode. Select alternate output function with GPIO_PCCFGH[7:4]
3	13	PC6	I/O	Digital I/O;
		OSC32B	I/O	32.768 kHz crystal oscillator Select analog function with GPIO_PCCFGH[11:8]
		nTX_ACTIVE	O	Inverted TX_ACTIVE signal (see PC5) Select alternate output function with GPIO_PCCFGH[11:8]
4	14	PC7	I/O	Digital I/O
		OSC32A	I/O	32.768 kHz crystal oscillator. Select analog function with GPIO_PCCFGH[15:12]
		OSC32_EXT	I	Digital 32 kHz clock input source
5	18	PA7	I/O High current	Digital I/O. Disable REG_EN with GPIO_DBGCFG[4]

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Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		TIM1_CH4	O	Timer 1 Channel 4 output Enable timer output with TIM1_CCER Select alternate output function with GPIO_PACFGH[15:12] Disable REG_EN with GPIO_DBGCFG[4]
			I	Timer 1 Channel 4 input. (Cannot be remapped.)
		REG_EN	O	External regulator open drain output. (Enabled after reset.)
6	19	PB3	I/O	Digital I/O
		TIM2_CH3	O	Timer 2 channel 3 output Enable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGL[15:12]
			I	Timer 2 channel 3 input. Enable remap with TIM2_OR[6].
		UART_CTS	I	UART CTS handshake of Serial Controller 1 Enable with SC1_UARTCFG[5] Select UART with SC1_MODE
		SC1SCLK	O	SPI master clock of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[6] Enable master with SC1_SPICFG[4] Select SPI with SC1_MODE Select alternate output function with GPIO_PBCFGL[15:12]
			I	SPI slave clock of Serial Controller 1 Enable slave with SC1_SPICFG[4] Select SPI with SC1_MODE
7	20	PB4	I/O	Digital I/O
		TIM2_CH4	O	Timer 2 channel 4 output Enable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGH[3:0]
			I	Timer 2 channel 4 input. Enable remap with TIM2_OR[7].
		UART_RTS	O	UART RTS handshake of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[7] Enable with SC1_UARTCFG[5] Select UART with SC1_MODE Select alternate output function with GPIO_PBCFGH[3:0]
		SC1nSSEL	I	SPI slave select of Serial Controller 1 Enable slave with SC1_SPICFG[4] Select SPI with SC1_MODE
8	21	PA0	I/O	Digital I/O
		TIM2_CH1	O	Timer 2 channel 1 output Disable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[3:0]
			I	Timer 2 channel 1 input. Disable remap with TIM2_OR[4].
		SC2MOSI	O	SPI master data out of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[4] Enable master with SC2_SPICFG[4] Select SPI with

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Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
				SC2_MODE Select alternate output function with GPIO_PACFGL[3:0]
			I	SPI slave data in of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
9	22	PA1	I/O	Digital I/O
		TIM2_CH3	O	Timer 2 channel 3 output Disable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[7:4]
			I	Timer 2 channel 3 input. Disable remap with TIM2_OR[6].
		SC2SDA	I/O	TWI data of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[6] Select TWI with SC2_MODE Select alternate open-drain output function with GPIO_PACFGL[7:4]
		SC2MISO	O	SPI slave data out of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[6] Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[7:4]
			I	SPI master data in of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
10	24	PA2	I/O	Digital I/O
		TIM2_CH4	O	Timer 2 channel 4 output Disable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[11:8]
			I	Timer 2 channel 4 input. Disable remap with TIM2_OR[7].
		SC2SCL	I/O	TWI clock of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[7] Select TWI with SC2_MODE Select alternate open-drain output function with GPIO_PACFGL[11:8]
		SC2SCLK	O	SPI master clock of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[7] Enable master with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[11:8]
			I	SPI slave clock of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
11	25	PA3	I/O	Digital I/O
		SC2nSSEL	I	SPI slave select of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
		TRACEC	O	Synchronous CPU trace clock Either disable timer output in

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Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		LK		TIM2_CCER or enable remap with TIM2_OR[5] Enable trace interface in ARM core Select alternate output function with GPIO_PACFGL[15:12]
		TIM2_CH2	O	Timer 2 channel 2 output Disable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[15:12]
			I	Timer 2 channel 2 input. Disable remap with TIM2_OR[5].
12	26	PA4	I/O	Digital I/O
		ADC4	Analog	ADC Input 4. Select analog function with GPIO_PACFGH[3:0].
		PTI_EN	O	Frame signal of Packet Trace Interface (PTI). Disable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[3:0].
		TRACEDATA2	O	Synchronous CPU trace data bit 2. Select 4-wire synchronous trace interface in ARM core. Enable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[3:0].
13	27	PA5	I/O	Digital I/O
		ADC5	Analog	ADC Input 5. Select analog function with GPIO_PACFGH[7:4].
		PTI_DATA	O	Data signal of Packet Trace Interface (PTI). Disable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[7:4].
		nBOOTMODE	I	Embedded serial bootloader activation out of reset. Signal is active during and immediately after a reset on NRST.
		TRACEDATA3	O	Synchronous CPU trace data bit 3. Select 4-wire synchronous trace interface in ARM core. Enable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[7:4]
14	29	PA6	I/O High current	Digital I/O
		TIM1_CH3	O	Timer 1 channel 3 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PACFGH[11:8]
			I	Timer 1 channel 3 input (Cannot be remapped.)
15	12	nRESET	I	Active low chip reset (internal pull-up)
16	30	PB1	I/O	Digital I/O
		SC1MISO	O	SPI slave data out of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select SPI with SC1_MODE Select slave with SC1_SPICR Select alternate output function with GPIO_PBCFGL[7:4]

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Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		SC1MOSI	O	SPI master data out of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select SPI with SC1_MODE Select master with SC1_SPICR Select alternate output function with GPIO_PBCFGL[7:4]
		SC1SDA	I/O	TWI data of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4] Select TWI with SC1_MODE Select alternate open-drain output function with GPIO_PBCFGL[7:4]
		SC1TXD	O	UART transmit data of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select UART with SC1_MODE Select alternate output function with GPIO_PBCFGL[7:4]
		TIM2_CH1	O	Timer 2 channel 1 output Enable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[7:4]
			I	Timer 2 channel 1 input. Disable remap with TIM2_OR[4].
17	31	PB2	I/O	Digital I/O
		SC1MISO	I	SPI master data in of Serial Controller 1 Select SPI with SC1_MODE Select master with SC1_SPICR
		SC1MOSI	I	SPI slave data in of Serial Controller 1 Select SPI with SC1_MODE Select slave with SC1_SPICR
		SC1SCL	I/O	TWI clock of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[5] Select TWI with SC1_MODE Select alternate open-drain output function with GPIO_PBCFGL[11:8]
		SC1RXD	I	UART receive data of Serial Controller 1 Select UART with SC1_MODE
		TIM2_CH2	O	Timer 2 channel 2 output Enable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGL[11:8]
			I	Timer 2 channel 2 input. Enable remap with TIM2_OR[5].
18	32	SWCLK	I/O	Serial Wire clock input/output with debugger Selected when in Serial Wire mode (see JTMS description, Pin 35)
		JTCK	I	JTAG clock input from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35) Internal pull-down is enabled
19	35	PC4	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
		JTMS	I	JTAG mode select from debugger Selected when in JTAG mode (default mode) JTAG mode is enabled after power-up or by

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Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
				forcing NRST low Select Serial Wire mode using the ARM-defined protocol through a debugger Internal pull-up is enabled
		SWDIO	I/O	Serial Wire bidirectional data to/from debugger Enable Serial Wire mode (see JTMS description) Select Serial Wire mode using the ARM-defined protocol through a debugger Internal pull-up is enabled
20	36	PB0	I/O	Digital I/O
		VREF	Analog O	ADC reference output. Enable analog function with GPIO_PBCFGL[3:0].
		VREF	Analog I	ADC reference input. Enable analog function with GPIO_PBCFGL[3:0]. Enable reference output with an ST system function.
		IRQA	I	External interrupt source A.
		TRACECLK	O	Synchronous CPU trace clock. Enable trace interface in ARM core. Select alternate output function with GPIO_PBCFGL[3:0].
		TIM1CLK	I	Timer 1 external clock input.
		TIM2MSK	I	Timer 2 external clock mask input.
21	34	PC3	I/O	Digital I/O Either Enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description)
		JTDI	I	JTAG data in from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35) Internal pull-up is enabled
22	33	PC2	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
		JTDO	O	JTAG data out to debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35)
		SWO	O	Serial Wire Output asynchronous trace output to debugger Select asynchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[11:8] Enable Serial Wire mode (see JTMS description, Pin 35) Internal pull-up is enabled
23	38	PC1	I/O	Digital I/O
		ADC3	Analog	ADC Input 3 Enable analog function with GPIO_PCCFGL[7:4]
		SWO	O	Serial Wire Output asynchronous trace output to debugger Select asynchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[7:4]
		TRACEDA	O	Synchronous CPU trace data bit 0 Select 1-, 2- or 4-wire synchronous

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Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		TA0		trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[7:4]
24	40	PC0	I/O High current	Digital I/O Either enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pin 35) and disable TRACEDATA1
		JRST	I	JTAG reset input from debugger Selected when in JTAG mode (default mode, see JTMS description) and TRACEDATA1 is disabled Internal pull-up is enabled
		IRQD (1)	I	Default external interrupt source D
		TRACEDATA1	O	Synchronous CPU trace data bit 1 Select 2- or 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[3:0]
25	43	PB5	I/O	Digital I/O
		ADC0	Analog	ADC Input 0 Enable analog function with GPIO_PBCFGH[7:4]
		TIM2CLK	I	Timer 2 external clock input
		TIM1MSK	I	Timer 2 external clock mask input
26	42	PB6	I/O High current	Digital I/O
		ADC1	Analog	ADC Input 1 Enable analog function with GPIO_PBCFGH[11:8]
		IRQB	I	External interrupt source B
		TIM1_CH1	O	Timer 1 channel 1 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PBCFGH[11:8]
			I	Timer 1 channel 1 input (Cannot be remapped)
27	41	PB7	I/O High current	Digital I/O
		ADC2	Analog	ADC Input 2 Enable analog function with GPIO_PBCFGH[15:12]
		IRQC (1)	I	Default external interrupt source C
		TIM1_CH2	O	Timer 1 channel 2 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PBCFGH[15:12]
			I	Timer 1 channel 2 input (Cannot be remapped)
28		GND	-	Ground
29		3.3V	I	DC3.3V supply
30				

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3.4. Power Mode Configuration

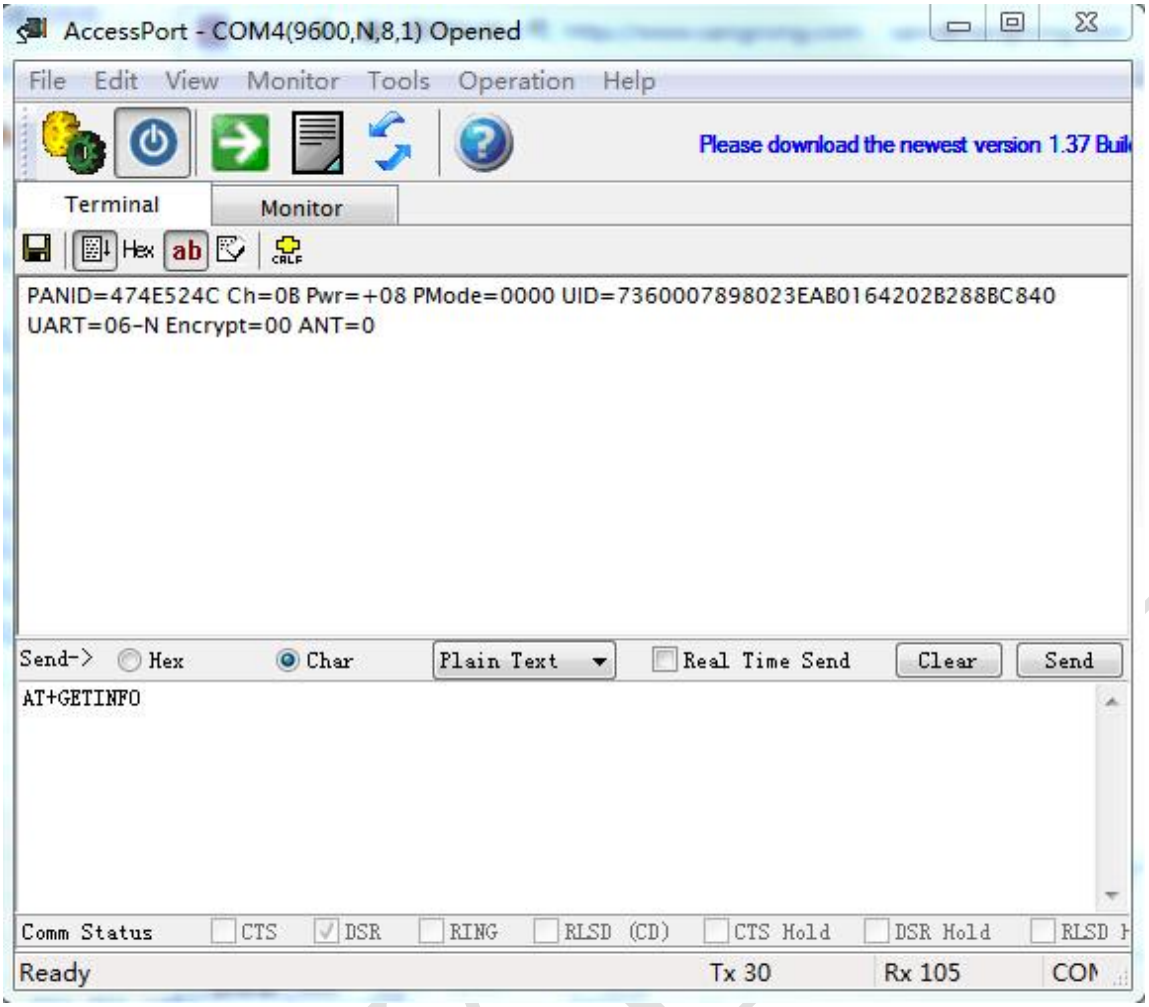
This part helps users to configure the power mode of RexBee module (currently only supports STM32W RexBee Module) through UART.

Users can refer to our AT commands manual to complete the UART configuration through serial port debugging software (such as AccessPort). The default UART baud rate of COO and HHU is set as 115200-8-N-1; Router set as 9600-8-N-1. The normal function of UART communication can be checked with command “AT+VER”. For more detailed AT commands, please refer to www.rexense.com

Acquire the current configuration information

Users can acquire the current configuration information of the module before UART debugging with command ‘AT+GETINFO’.

REXENSE



The return data includes basic configuration info of module :

Pwr=+08 : means TX is +8dBm ;

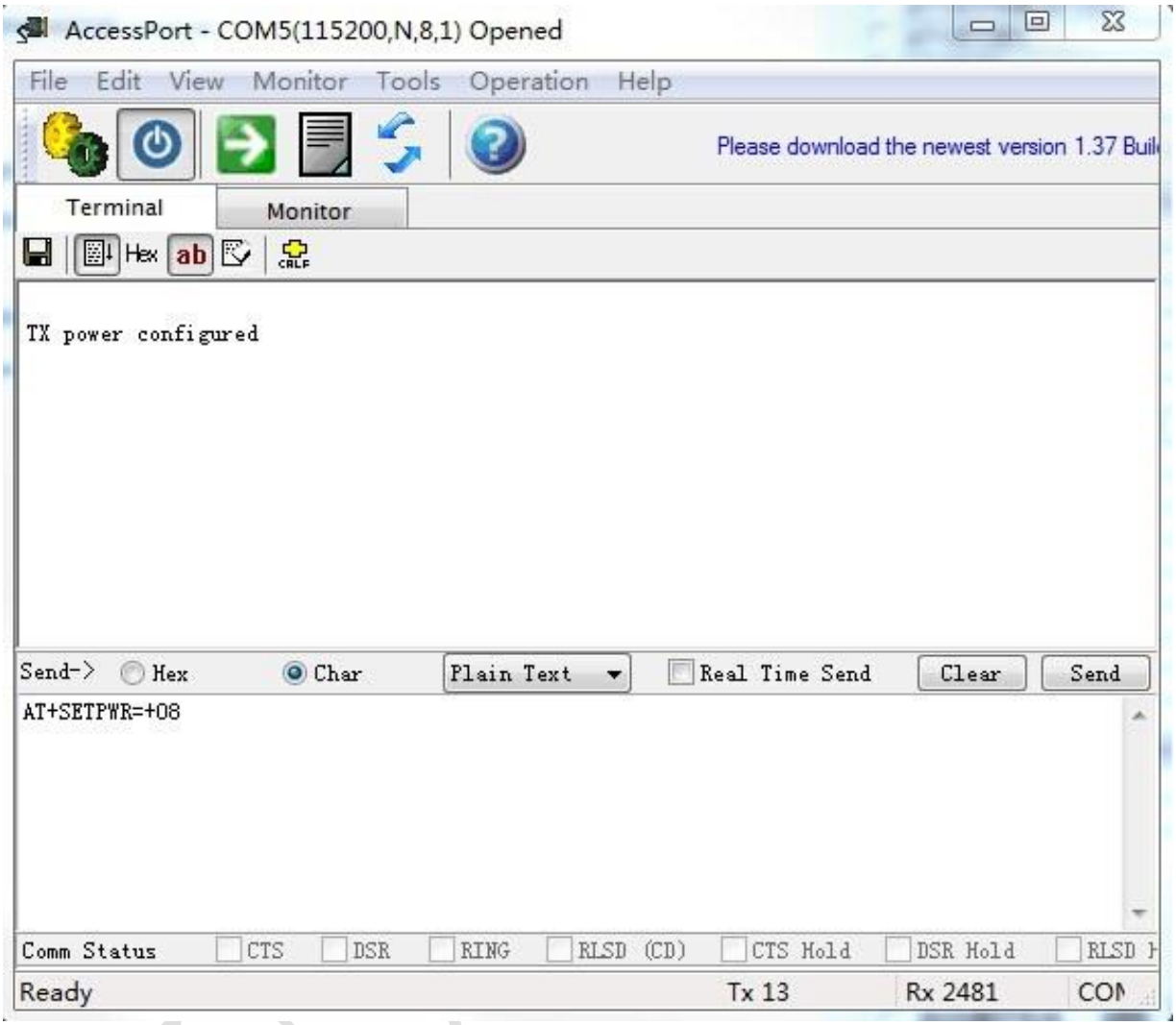
PMode=0000 : means power mode is standard mode.

Important Note :

1. **For standard RexBee module**, the TX power of the wireless chip means the TX power of the module.

- It is recommended that the TX power set as +08dBm to have better communication performance.

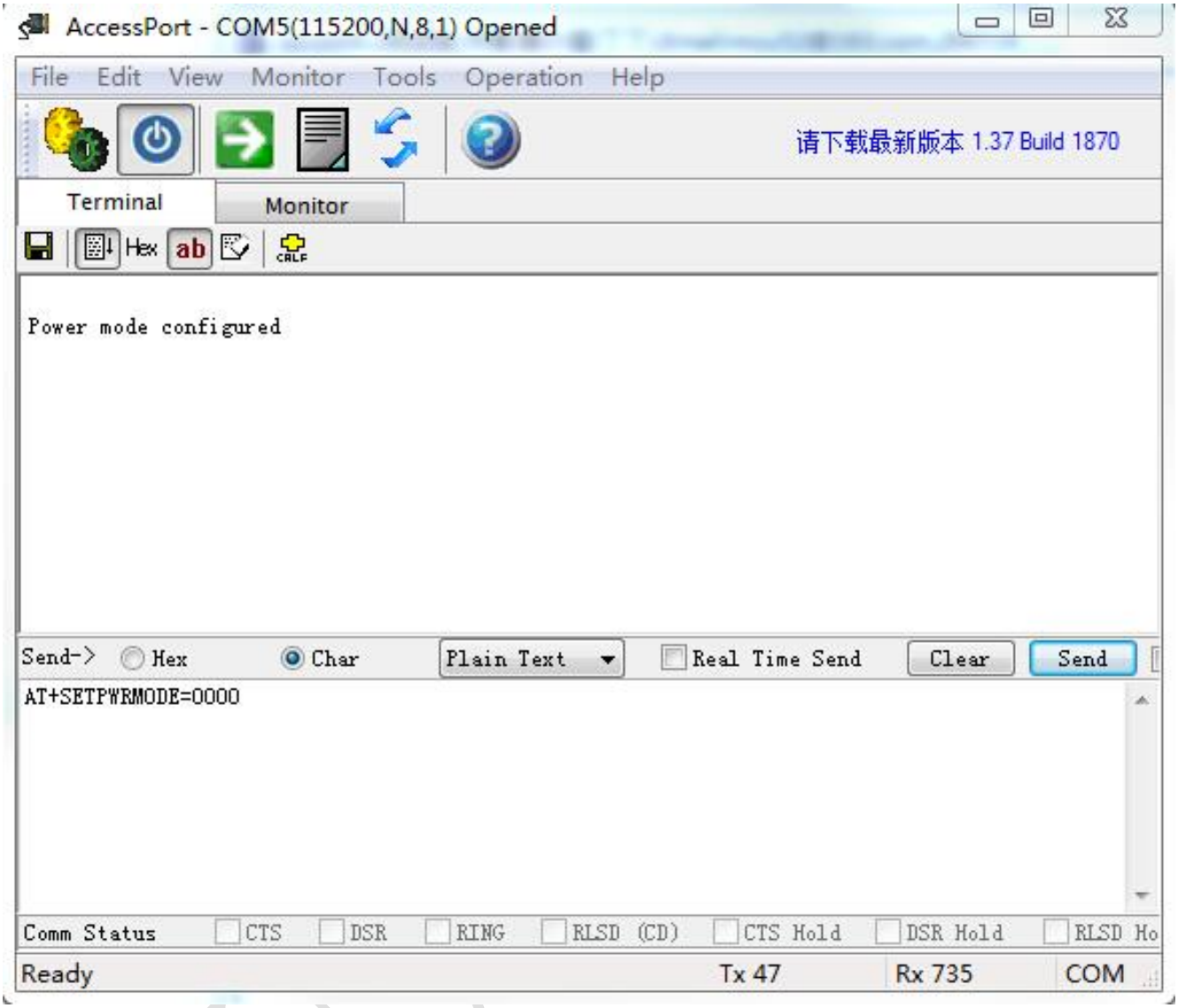
- The TX power of the wireless chip can be configured with the command “AT+ SETPWR”.



2. **For enhanced RexBee module,** the TX power of the wireless chip amplified by the power amplifier (PA) means the TX power of the module。

- Standard RexBee module works in **standard power mode** configured by the command below :

AT+SETPWRMODE=0000

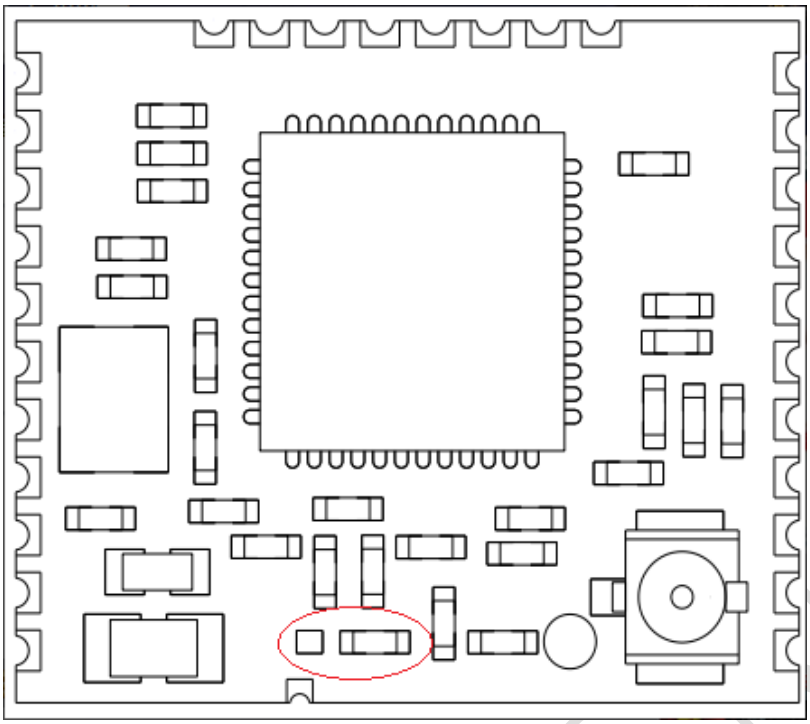


3.5 Antenna Specifications

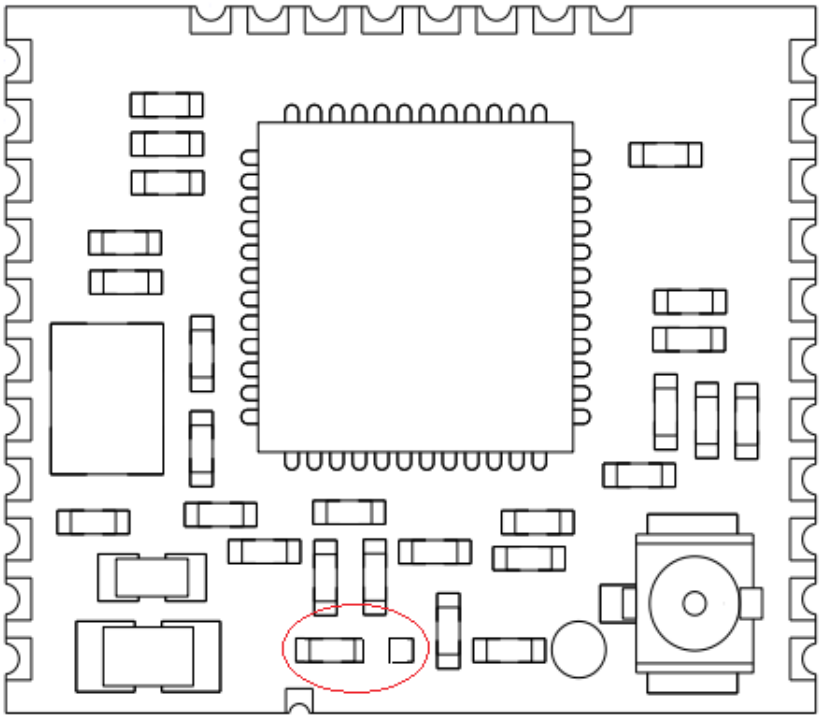
REX3U has 2 antennas, buyer need to confirm with sales about the type before purchasing.

Figure 3-11. Jumper indication

Use PCB antenna：



Use other 3 exterior antenna：



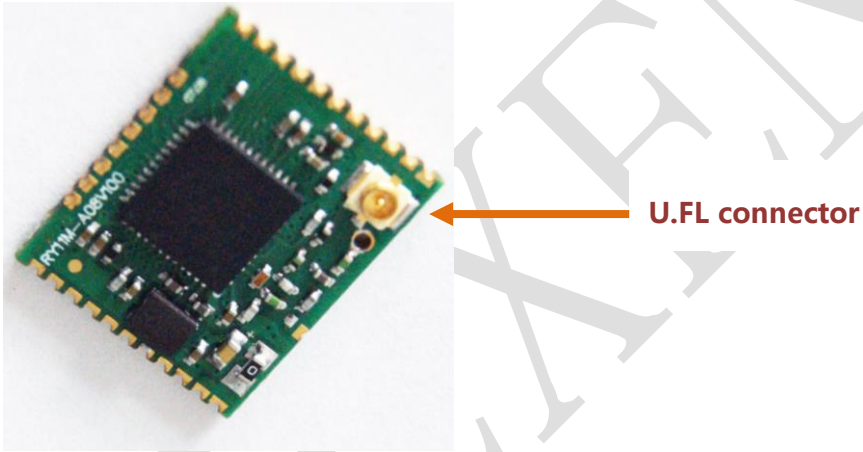
REXENSE

3.5.1 Simple antenna

Figure **3-12. simple**

3.5.2 U.FL connector

Figure **3-13. U.FL connector**



Remark：Note: when the U.FL (IPEX) connector is used, it's necessary to use the antenna cable and the SMA antenna at the same time. Please see the pictures below.

Figure **3-14. antenna cable**

Cable (AN11): length(11cm)，insert loss(1dBi)

Picture **3-15. SMA antenna**

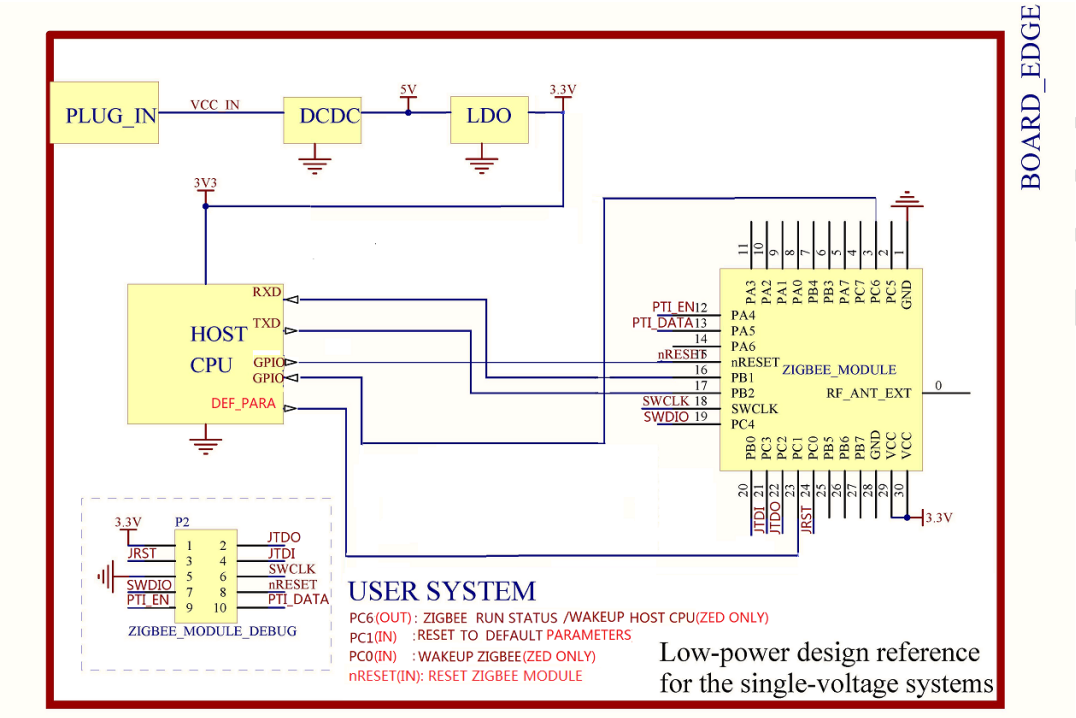
SMA antenna (AN2400): gain(2dBi)

Picture **3-16. Completing picture**

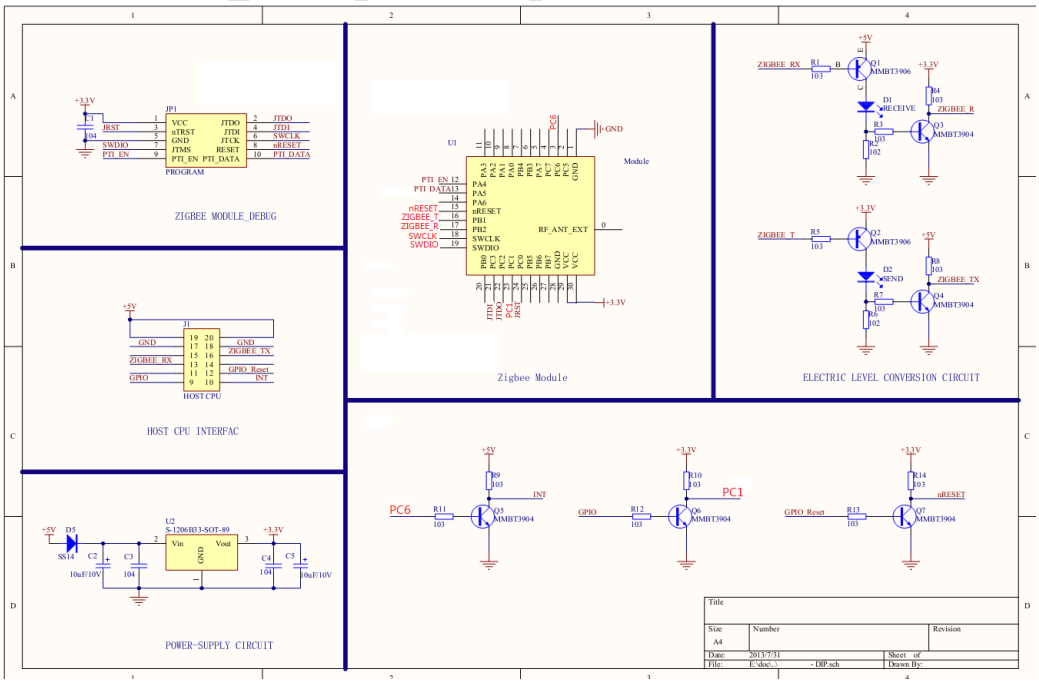
REXENSE

3.6. Module Circuit Reference Design

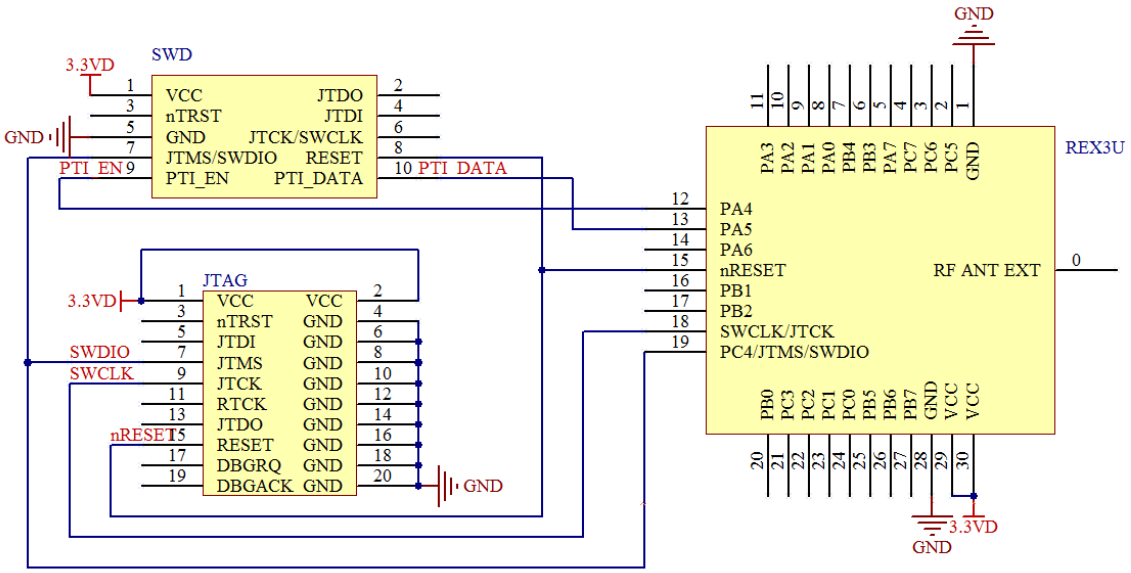
3.6.1. When system voltage is 3.3V



3.6.2. When system voltage is 5.0V

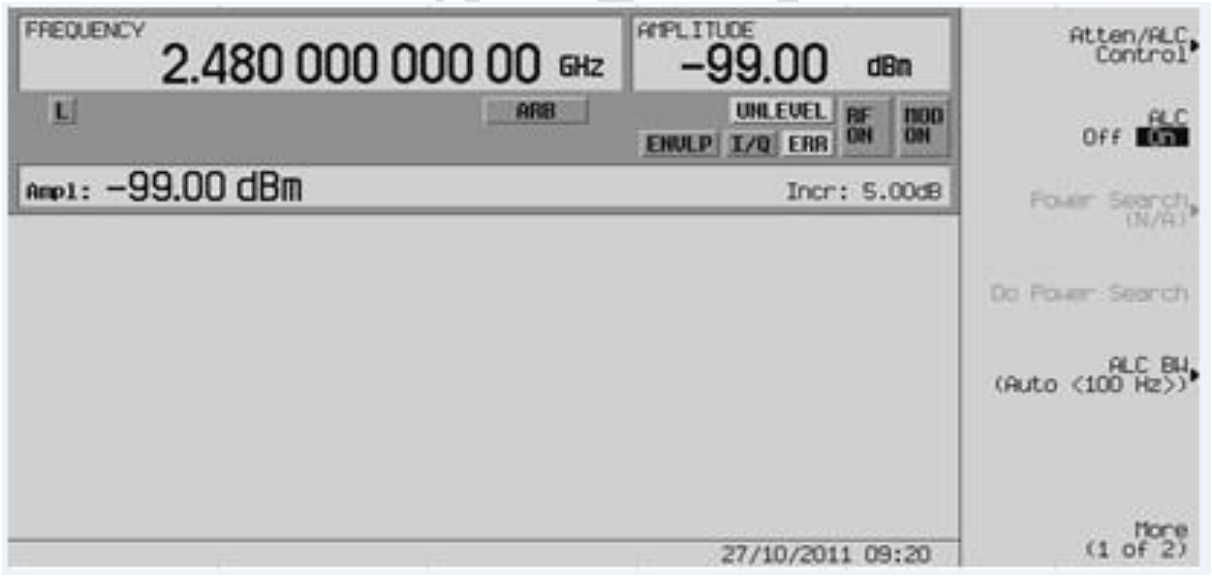


3.7. Module Debug and Program Interface connection



3.8. Test Result of RF Performance

Figure 3-17. RX sensitivity



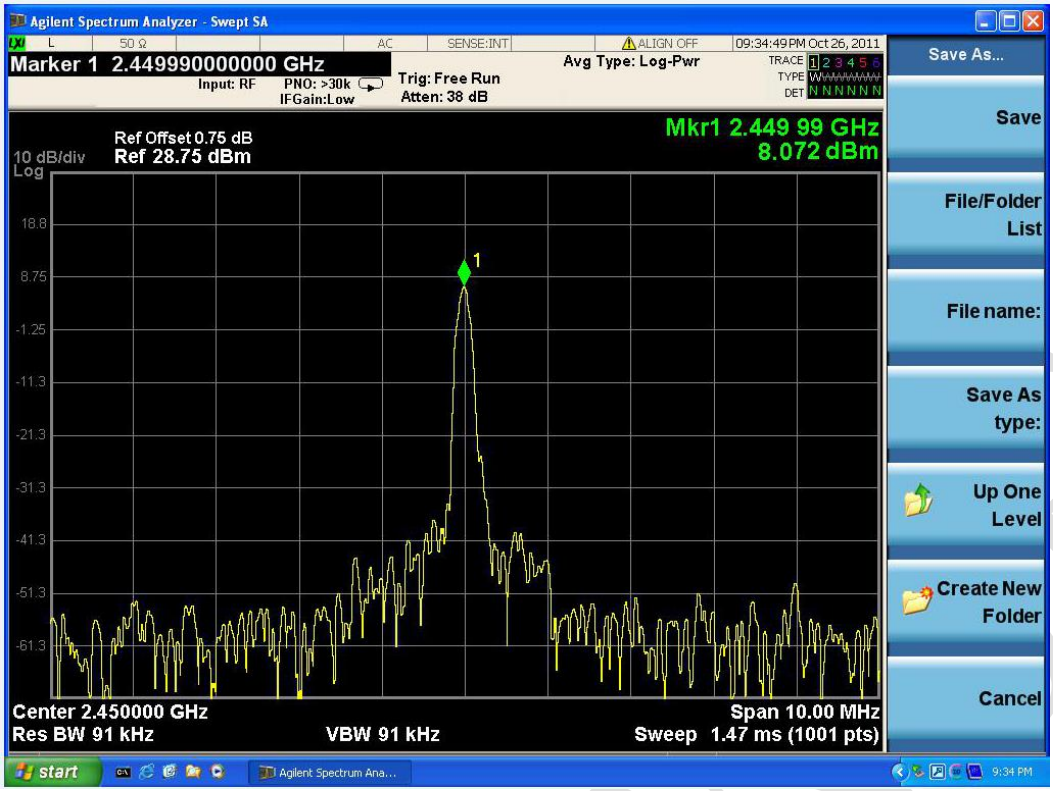


Figure 3-18. Modulating Signal Testing

请登录官网或致电 官方网站：www.rexense.cn 24小时服务热线：86-571-85395623

4. Ordering Information

REX 3 D 57 U

Manufacturer

REX=REXENSE

Serial

3=Zigbee serial (Cortex™-M3 Core)

Package type

D=DIP

S=SMD

U=Ultra compact

L=LED lighting

Chip No.

51=EM351

57=EM357 (default)

64=STM32W108CBU64

Antenna

U=U.FL connector (default)

B=PCB antenna

L=L antenna

P=Pin out

S=SMA antenna

H=Spring antenna

REXENSE

5. Contact Us

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